AXIENT

Developing a CubeSat Payload Interface Board for Neuromorphic Processing and Distributed Computing

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NASA Small Spacecraft Technology Program (SST) & Axient

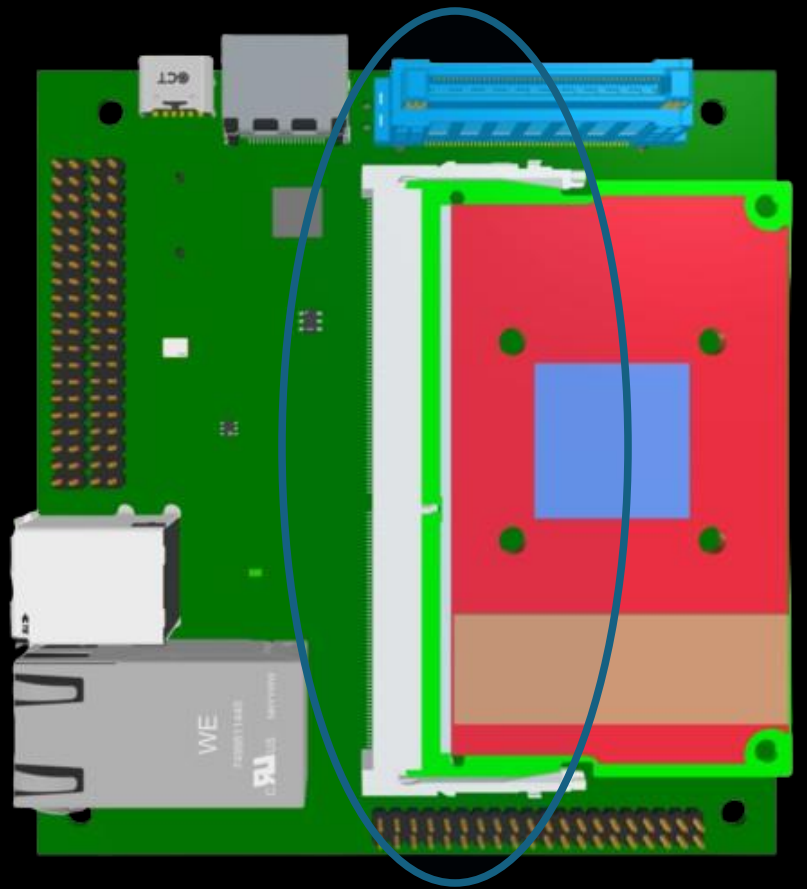
Interface Board Objective

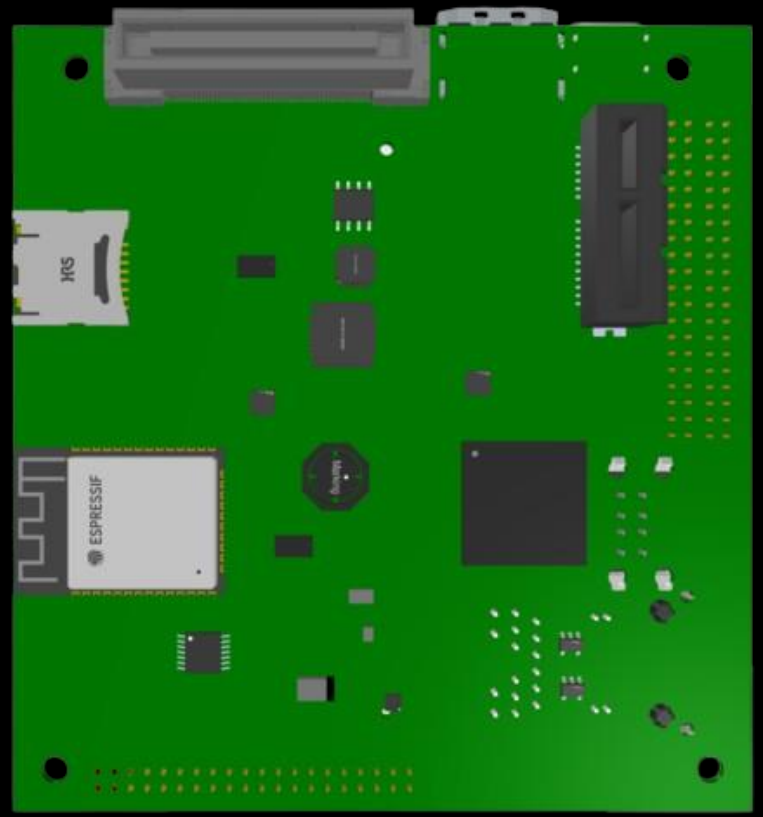
The NASA Small Spacecraft Technology Program is interested in testing low cost and low power processors for future technology demonstrations.

Project objective: develop a platform to explore and test low power on-board data processing technologies.

- Ground testing for initial verification
- Further maturation may include:
  - Suborbital balloon launch
  - LEO technology demonstration

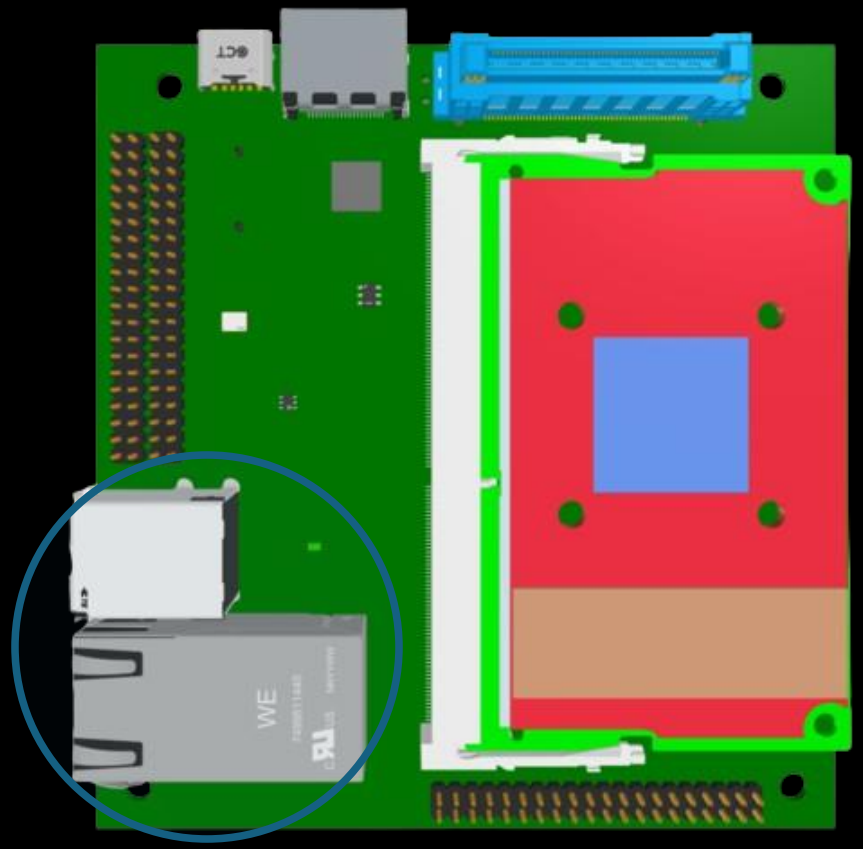
Host Processor Compatibility

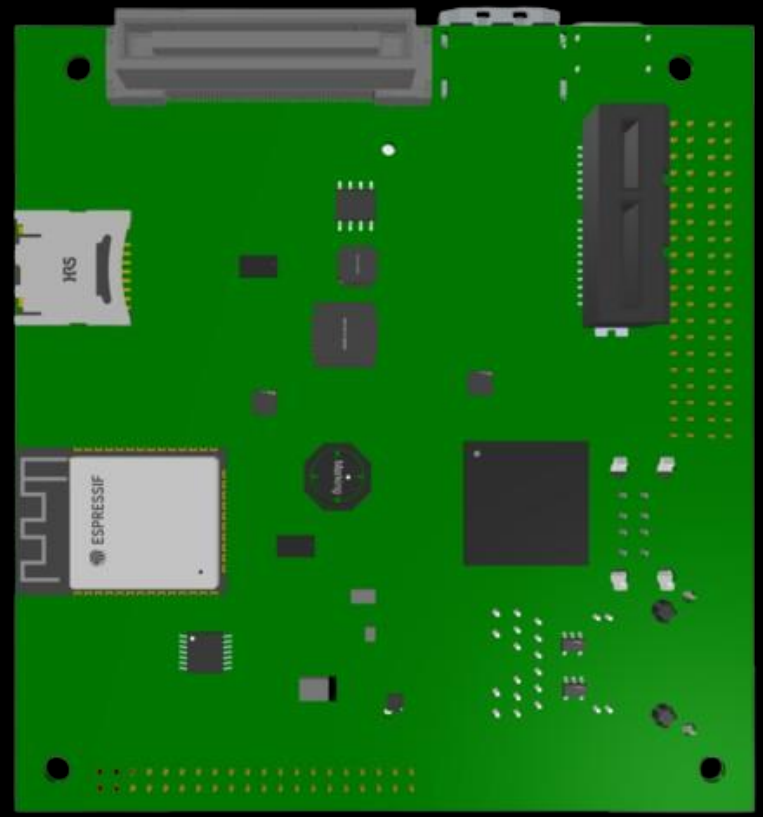




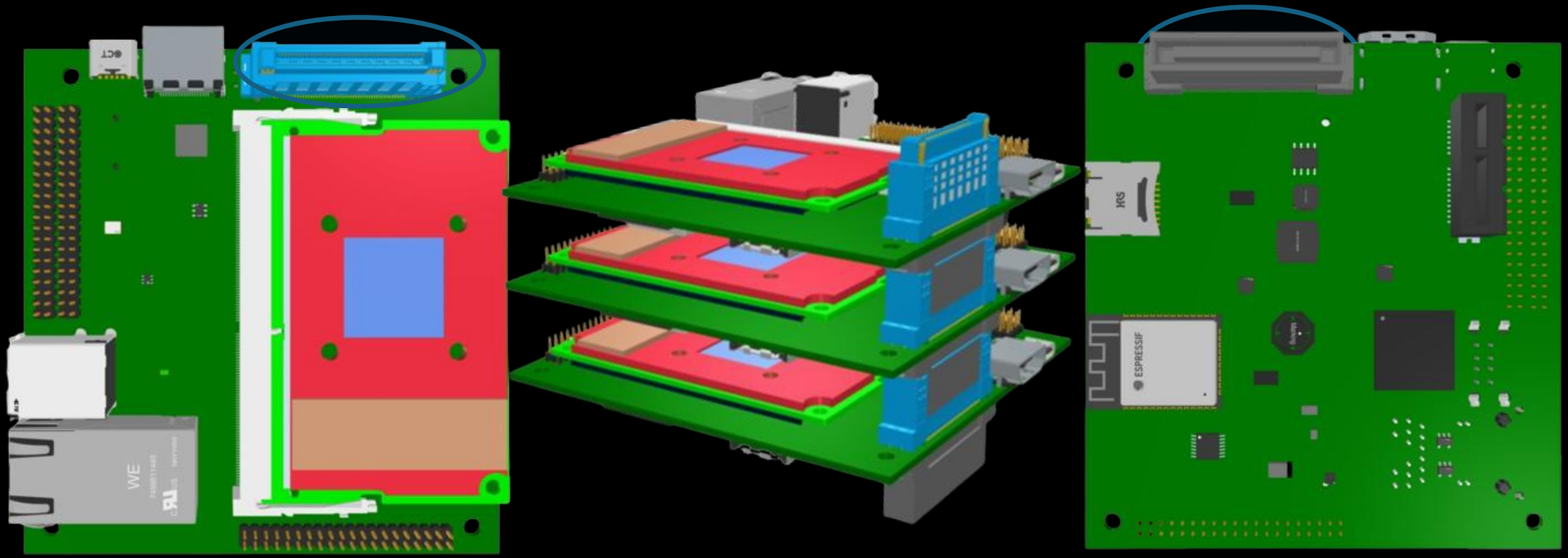
Host Processor Demonstration

Neuromorphic Co-Processors

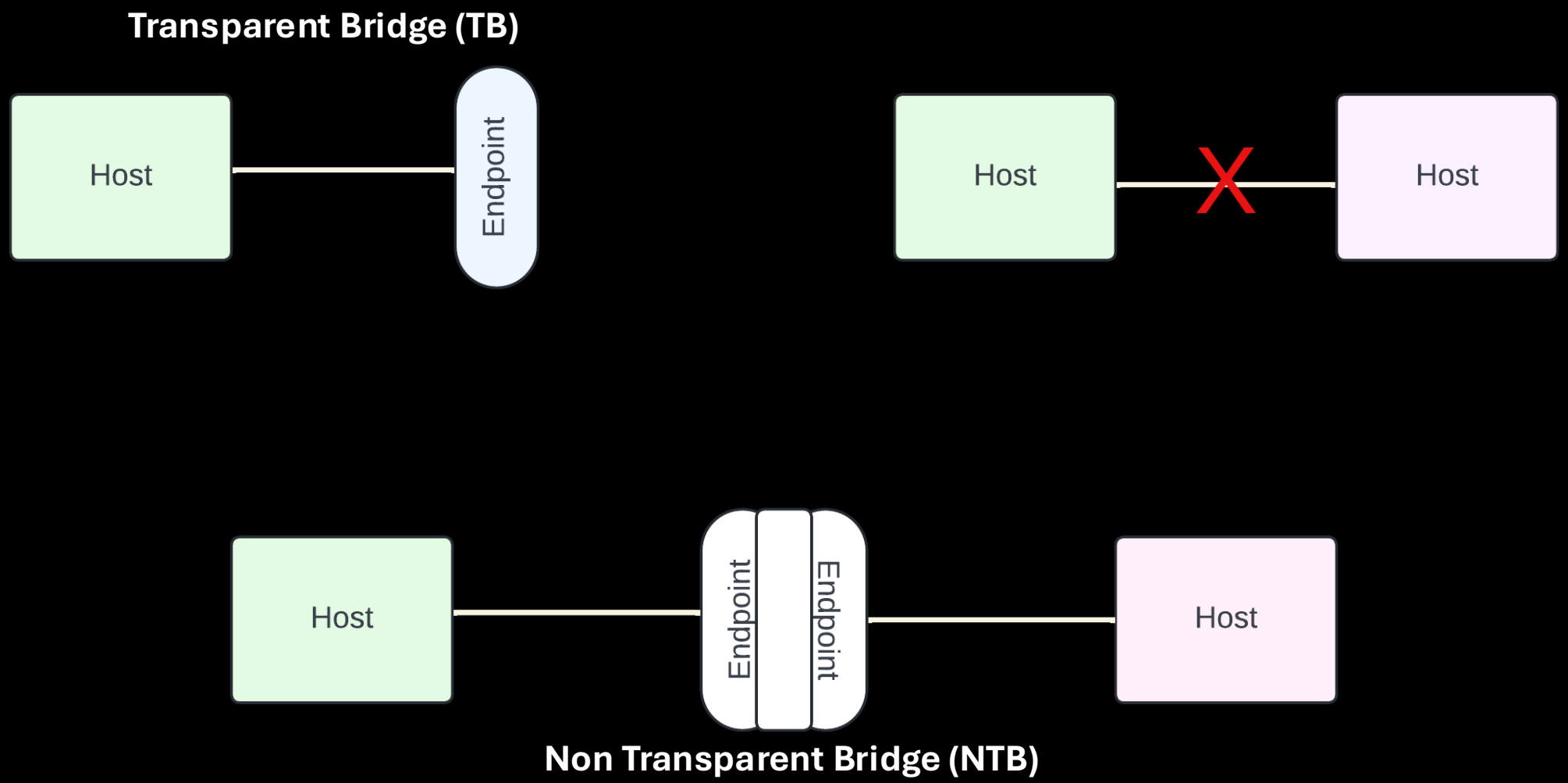


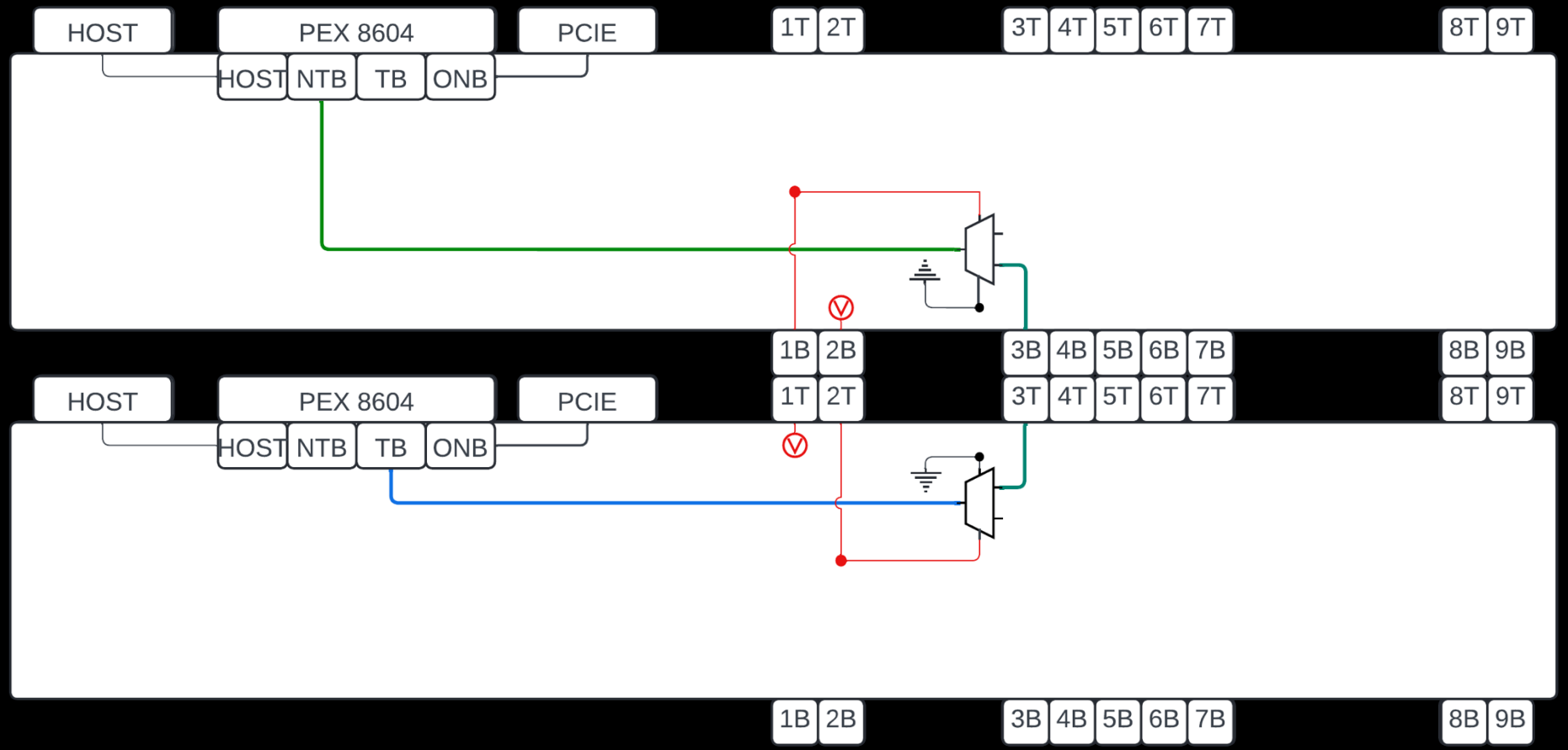


Distributed Computing



Backplane-less PCIE Stack

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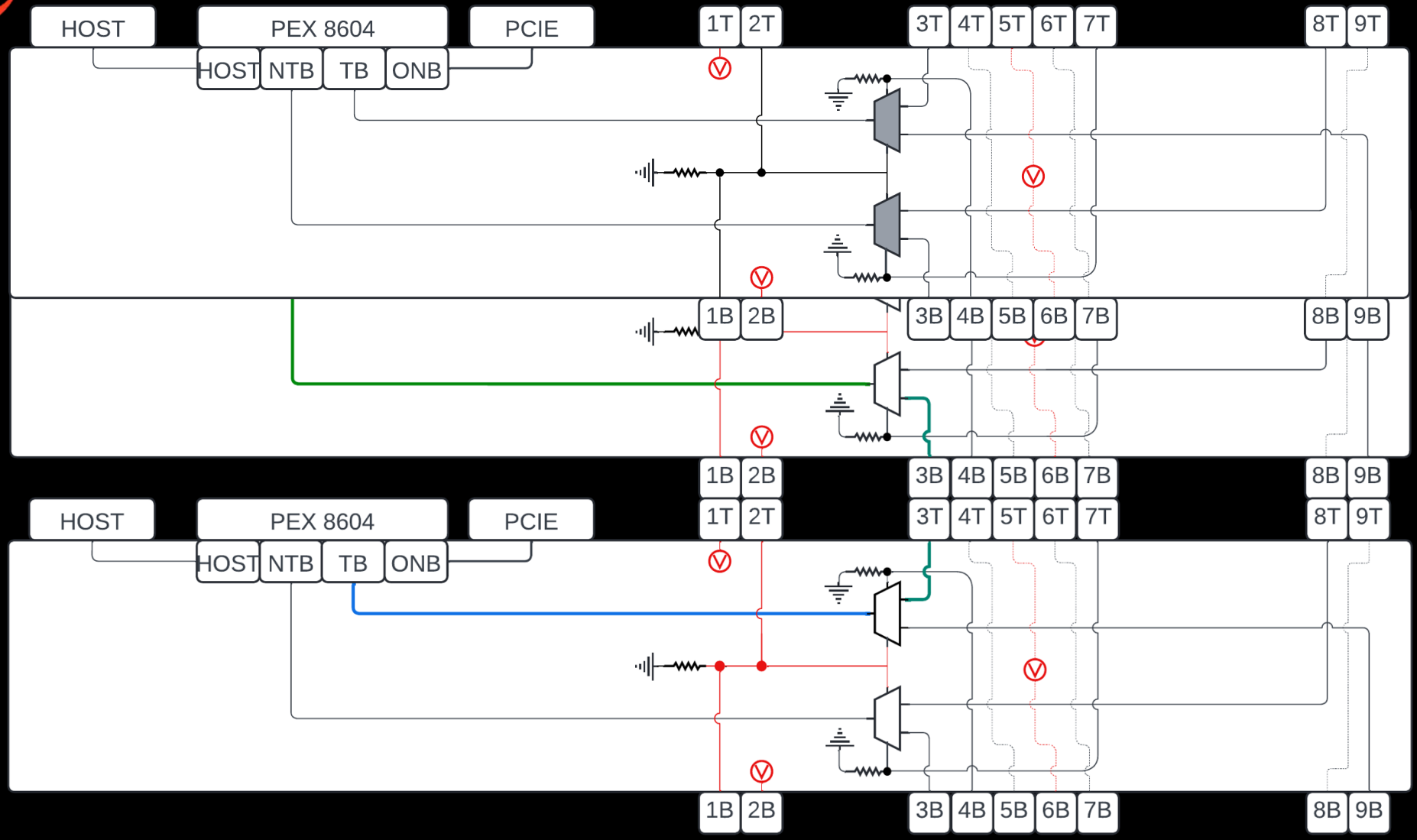
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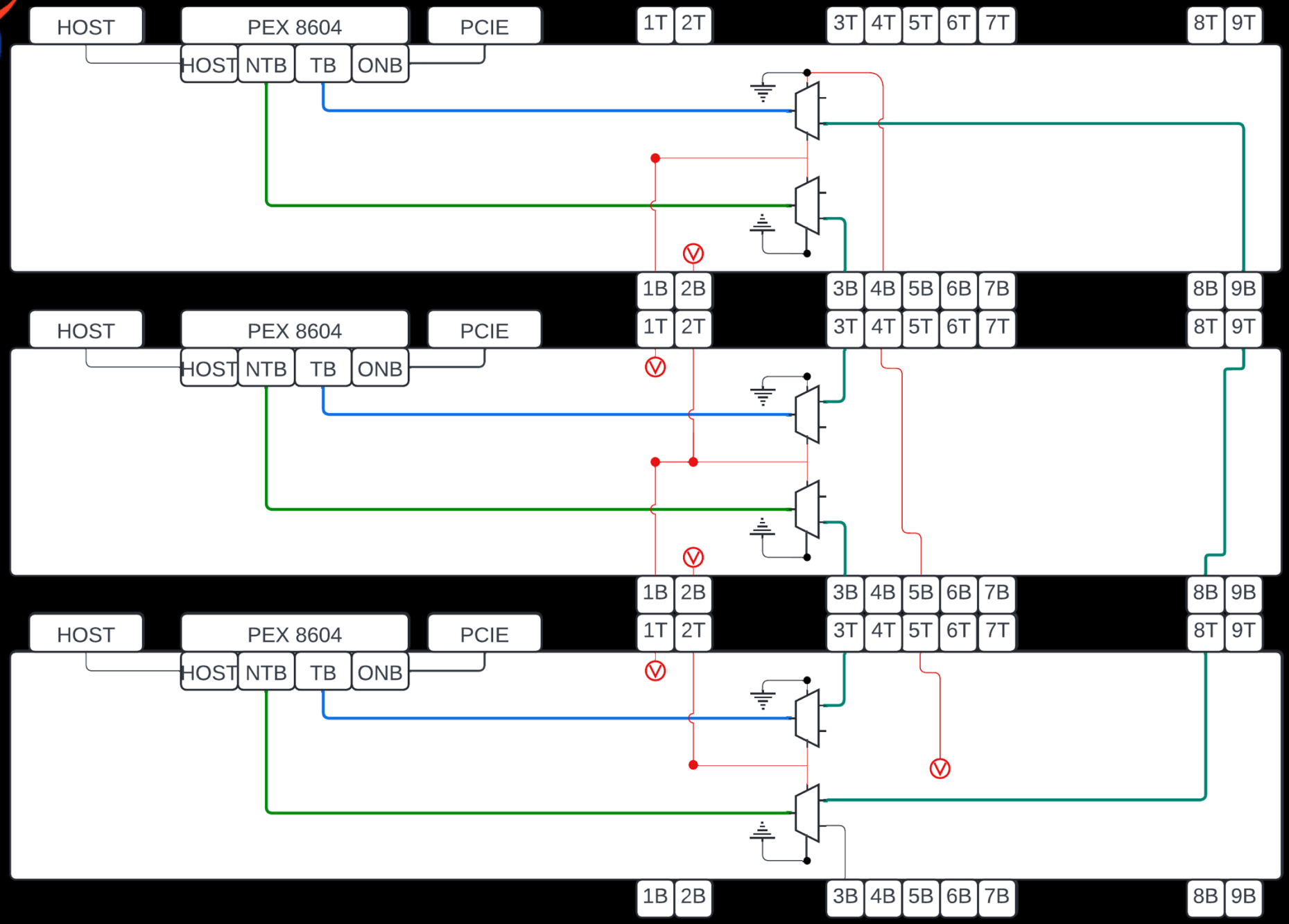
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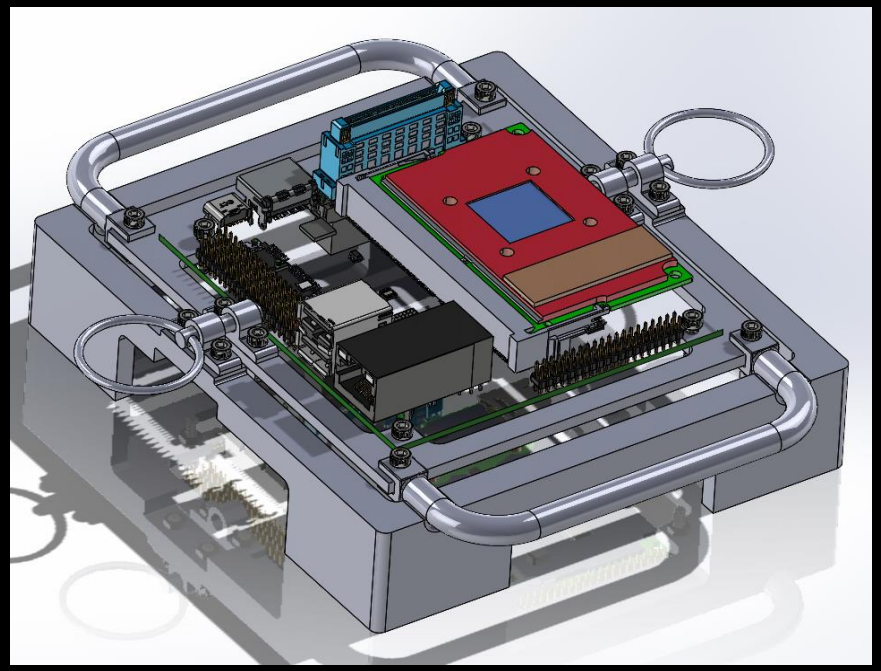
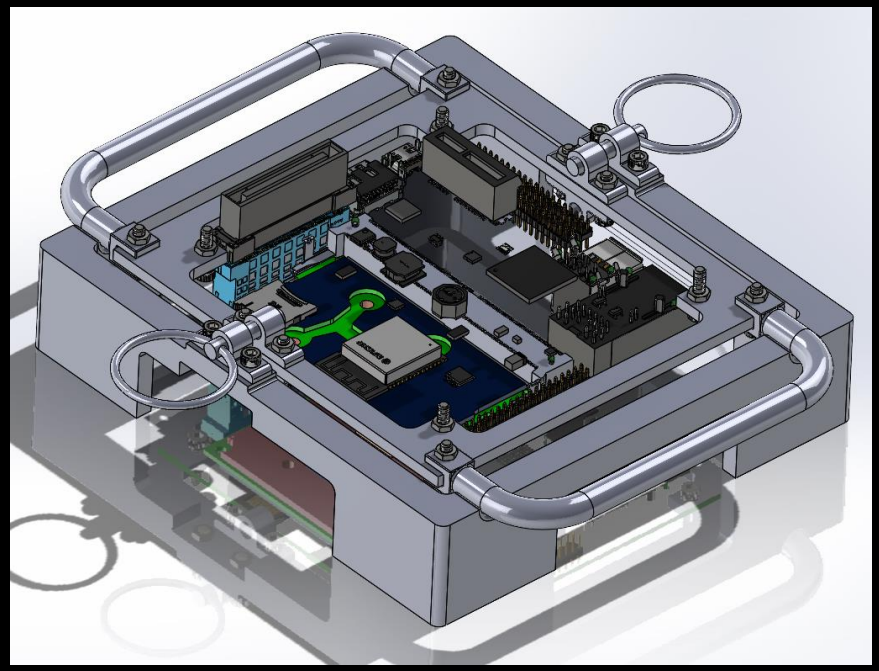
Interface Board Bringup

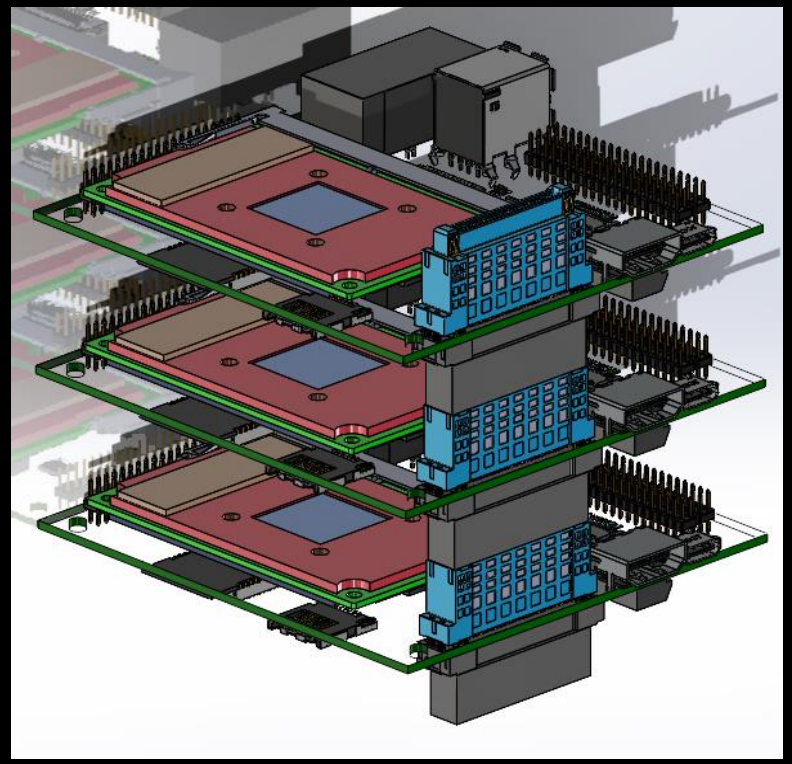
- Single-board bringup
- "Flipping" test fixture allows rotation of board to test both sides

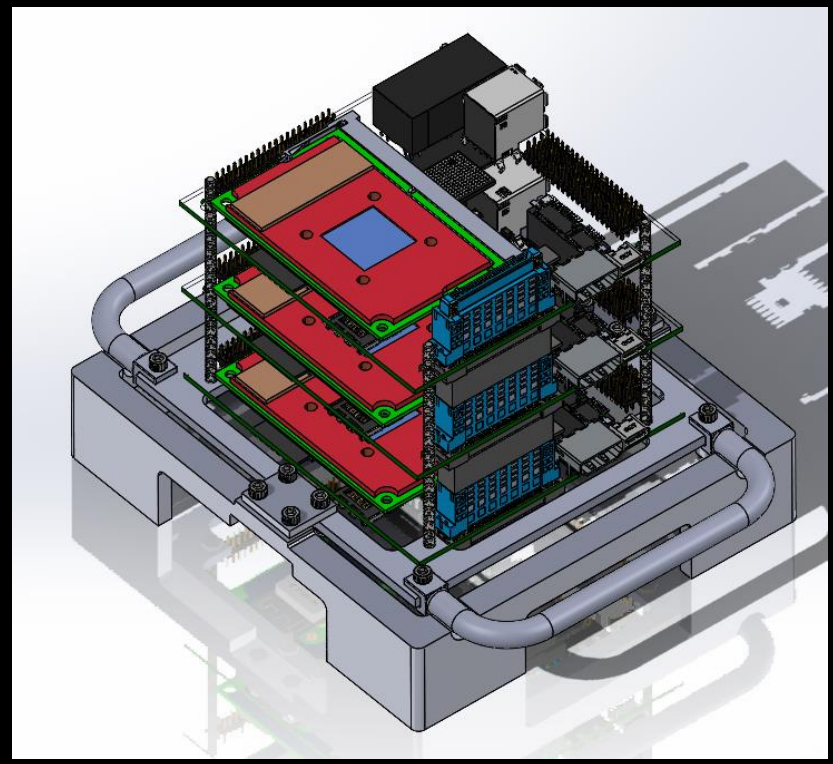




Interface Board Bringup

- Tests of stacked boards to verify distributed computing
- "Stack" test fixture simulates board stack in CubeSat bus





Thermal Analysis and Heat-Sink Design

- Interface board stack will likely need heat sinks to the structure
- Upcoming analysis with Thermal Desktop to determine heat dissipation possible
- Ensure that boards never exceed operation and survivability temperature ranges for main power consumers

Structure

- Preliminary 2U structure design
- Intended for weather balloon suborbital testing and LEO technology demonstration