X-57
Maxwell

High Lift Propeller Indicator and Control Requirements Document

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1 Scope

This document establishes the interface requirements for the X-57 High Lift Propeller Control (HiPC) and the High Lift Propeller Indicator (HiPI) subsystems.

2 System Description

The HiPI and HiPC shall follow the A/B system architecture for the X-57 aircraft. The A/B architecture is utilized by flight critical systems including the high lift propulsors (high lift propeller, high lift motor and high lift motor controller). This architecture provides redundancy in the event of an A system failure or a B system failure. The A and B high lift propulsors are distributed across the left and right wing so that a failure of an A system or B system will not produce an abrupt asymmetric thrust event and cause an adverse yaw condition for the aircraft. See **Figure 1** for the high lift propulsors distribution on the wing.

The HiPI and HiPC provide the indication and control interfaces between the X-57 cockpit and the 12 High lift motor controllers (HLMCs). **Figure 2** provides a block diagram of this system.

Six HLMCs on the A system will provide controller status inputs to HiPI-A and six HLMCs on the B system will provide controller status inputs to HiPI-B. HiPI-A and HiPI-B will process these controller inputs to provide the status of all 12 HLMCs to the pilot and ground crew indicators in the cockpit. HiPC-A will process and distribute commands from the cockpit to the six HLMC on the A system and HiPC-B will process and distribute commands from the cockpit to six HLMCs on the B system.

The cockpit provides commands to the HiPC using an Arm/Disarm switch that arms and disarms the HLMCs and a Mode switch that places the HLMCs in an Airspeed or Fixed Control Mode. The Airspeed Mode varies motor RPM with Airspeed. The Fixed Mode commands the motor to a fixed or constant RPM. There is also a yoke mounted disarm switch which allows the pilot to quickly disarm the HLMCs. If the yoke mounted disarm switch is engaged by the pilot, the HLMCs will disarm and stay disarmed. An indicator will notify the pilot that the HLMCs are disarmed but the Arm/Disarm switch is still in the Arm position. This indicator will turn off when the pilot places the Arm/Disarm switch in the Disarm position.

HiPC-A, HiPC-B, HiPI-A and HiPI-B will each have an independent circuit breaker in the cockpit providing power. This will isolate the power to each unit and prevent a power fault in one unit causing a power fault in the remaining units.

2.1 System Diagram

High Lift Motor and High Lift Motor Controller distribution across the Mod III/IV wing is shown in **Figure 1**

Figure 1 – High Lift Propulsor Distribution

A functional block diagram and interfaces for HiPI and HiPC is shown in **Figure 2**

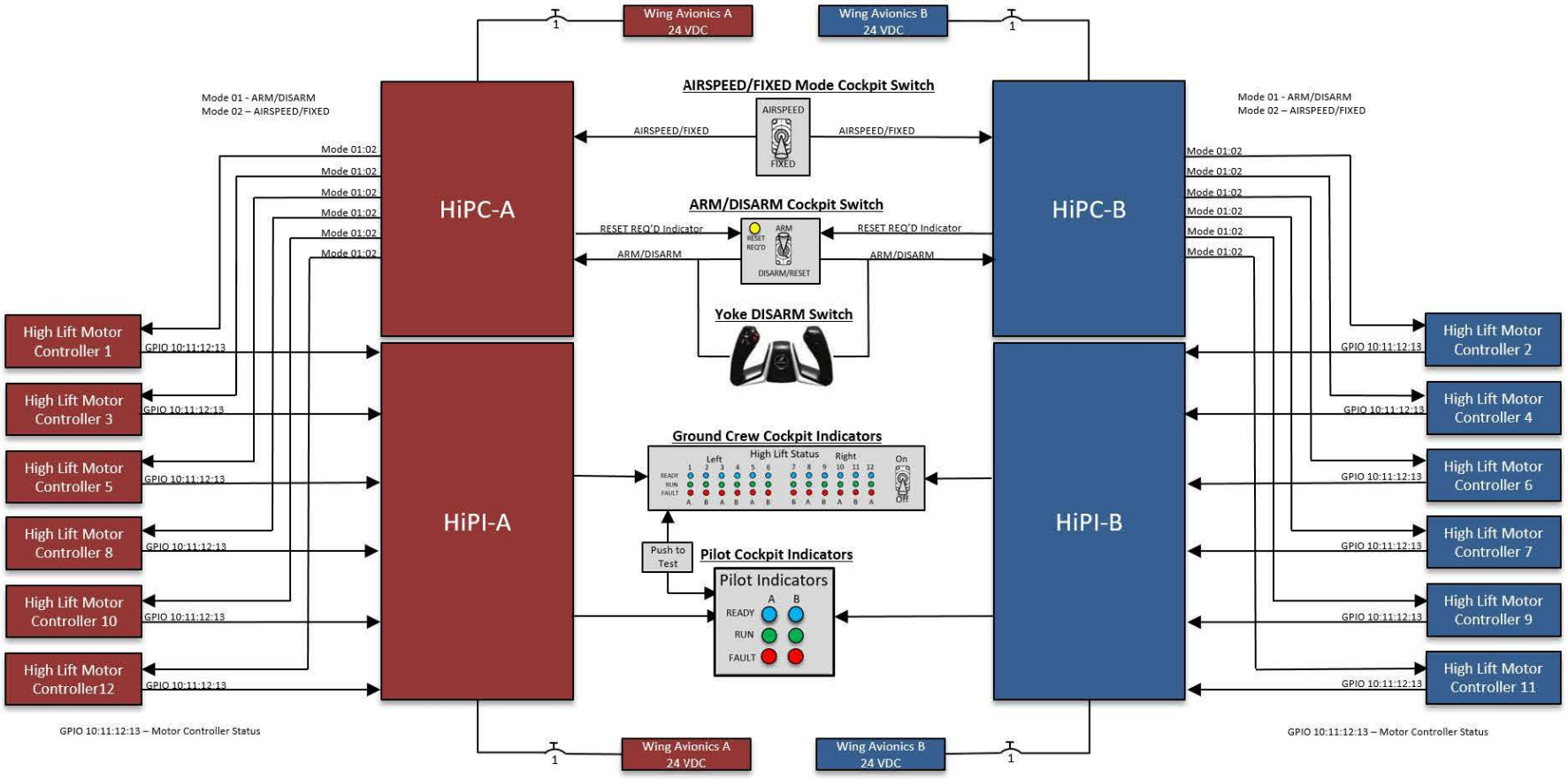

Figure 2 – HiPI & HiPC Block Diagram with Interfaces

3 Applicable Documents

The following documents were used to assist in the development of the requirements specified in this document

a. ETP-CEPT-007, Environmental Test Plan
b. REQ-CEPT-018, High lift Motor Controller Hardware Requirements Document
c. QAP-CEPT-008, Quality Assurance Plan
d. ANLYS-CEPT-023, Analysis of X-57 High lift Propeller Operating Conditions
e. ANLYS-CEPT-032, Mod IV Avionics Power Analysis
f. ICD-CEPT-006, Cockpit ICD

4 Requirements Standards

The following format was used to develop the requirements.

- Requirements are in the form “who shall do what”.
- Requirements use the proper terminology:
  - “Shall” is used to denote a binding requirement.
  - “Will” is a statement of fact or declaration of purpose.
  - “Should” is used to denote an optional goal.
- Requirements are clear, concise, and unambiguous.
- Requirements are verifiable through inspection, analysis, test, or demonstration.
- Rationale is provided as a means to capture the purpose of the requirement. Its intent is to aid the reader in understanding the requirements. The rationale does not contain any requirements; therefore, no verification of the rationale is required.

5 Requirements Verification Methods

Requirement verification methods are not under configuration control, and may be changed by the requirement owner, with agreement from the associated IPT. The actual verification method used to close a requirement is documented in the requirements verification sheet.

The requirement verification methods employed are inspection, analysis, test, and demonstration. The following sections define the verification methods used.

5.1 Verification Method - Inspection

Inspections determine conformance to requirements by the visual examination of drawings, data, or the item itself using standard quality control methods, without the use of special laboratory procedures or equipment. Inspection includes examining a direct physical attribute such as dimension, weight, physical characteristics, color or markings.

5.2 Verification Method - Analysis

Analysis is the evaluation of data by generally accepted analytical techniques to determine that the item will meet specified requirements. Analysis is selected as the verification activity when test or demonstration techniques cannot adequately or cost effectively address all the conditions under which the system must perform, or the system cannot be shown to meet the requirement without analysis.

5.3 Verification Method - Test

Test is a verification method in which technical means, such as the use of special equipment, instrumentation, simulation techniques, or the application of established principles and procedures are used for the evaluation of the system or system components to determine compliance with requirements. Test consists of operation of all or part of the system under a limited set of controlled conditions to determine the quantitative design or performance requirements have been met. Tests may rely on the use of elaborate instrumentation and special test equipment to measure the parameters that characterize the requirements.

The analysis of data derived from tests is an integral part of the test program and should not be confused with “analysis” as defined earlier. Testing is the preferred method of verification when:

- Analytical techniques do not produce adequate results
- Failure modes exist which could compromise personnel safety, adversely affect flight systems or result in a loss of mission objective
- Components are directly associated with critical system interfaces

5.4 Verification Method - Demonstration

Verification by demonstration shows that an end product meets the performance or operational requirement in a qualitative manner. It is used for determination of properties of an end item or component by observation of its operation or characteristics. It is generally a basic confirmation of performance capability, differentiated from testing by the lack of detailed data gathering.

6 High Lift Propeller Control (HiPC) Requirements

6.1 HiPC Interface Requirements

These requirements apply to HiPC-A and HiPC-B. Please refer to **Figure 2** for the HiPC-A and HiPC-B interface boundaries

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HiPC ARM Command					
HIPC.1	The HiPC shall provide an Arm signal to the HLMCs when the ARM/DISARM switch in the cockpit is moved from the DISARM position to the ARM position.	A pilot selectable switch is used to Arm and Disarm the High Lift System.	Demonstration	C.3.1.1	HR-30 Cause H, HR-31 Cause R HR-31 Cause R, Mit 31
HIPC.1.1	The HiPC Arm signal from the ARM/DISARM switch in the cockpit shall be a closed circuit.	A closed circuit will prevent the accidental arming of the HLMC by an open circuit caused by a broken wire or unmated connector. Disarm is the failsafe condition for the HLMCs.	Test	HIPC.1	See HIPC.1
HIPC.1.1.1	The HiPC Arm closed circuit from the ARM/DISARM switch in the cockpit shall have a resistance of less than 10 Ω as measured at the Arm input to the HiPC.	10 Ω of resistance is adequate resistance to indicate a closed circuit. This would include wire resistance, connector resistance switch closure resistance plus margin.	Test	HIPC.1.1	See HIPC.1
HIPC.1.2	The HiPC Arm voltage output signal provided to the HLMC shall reference the HiPC power return	The LCA715STR opto-isolator in the HLMC is a single ended device and does not accept a differential signal.	Test	HIPC.1	See HIPC.1

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC.1.2.1	The HiPC Arm voltage output signal provided to the HLMC shall range between 14 VDC to 16 VDC	A voltage must be applied to the HLMC input to Arm the motors and start the motors spinning. This will prevent the motors from spinning due to a loss of voltage. The HLMC has 630 ohms in series with the LCA715STR opto-isolator LED to activate the ARM command. 14 VDC will continually source 20.3ma into the LED. 16 VDC will continually source 23.5ma. The minimum current required to activate the opto-isolator LED is 1ma to 5ma. Peak current is 50ma continuous or 1amp for 10ms. 20 to 25ma will provided a robust signal to activate the LED for the ARM command.	Test	HIPC.1.2	See HIPC.1
HIPC.1.2.1.1	The HIPC Arm signal shall have a current limit of 30 ma	The output current must below the peak input current for the LCA715STR opto-isolator LED.	Test	HIPC.1.2.1	See HIPC.1
HiPC DISARM Command					
HIPC.2	The HiPC shall provide a Disarm signal to the HLMCs when the ARM/DISARM switch in the cockpit is moved from the ARM position to the DISARM position.	A pilot selectable switch is used to Arm and Disarm the High Lift System.	Demonstration	C.3.1.4	HR-30.2 Mit. 8 HR-30.1 Mit. 13, HR-30 Cause H, J, Mit. 13
HIPC.2.1	The HiPC Disarm signal from the ARM/DISARM switch in the cockpit shall be an open circuit.	The default condition for the HLMC is Disarm. An open circuit caused by a broken wire or an unmated connector will default the HLMC to the Disarm. This is a “fail safe” condition.	Test	HIPC.2	See HIPC.2

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC.2.1.1	The HiPC Disarm open circuit from the ARM/DISARM switch in the cockpit shall have a resistance of at least 100k Ω as measured at the Disarm input to the HiPC.	More than 100k Ω of resistance is adequate to indicate an open circuit.	Test	HIPC.2.1	See HIPC.2
HIPC.2.2	The HiPC Disarm signal provided to the HLMC shall be a voltage referenced to the HiPC power return.	The LCA715STR opto-isolator in the HLMC is a single ended device and does not accept a differential signal.	Test	HiPC.2	See HIPC.2
HIPC.2.2.1	The HiPC Disarm signal voltage to the HLMC shall be less than 1.6 VDC.	0 VDC will replicate an open wire or loss of voltage and will cause the HLMC to disarm. This is a "fail safe" condition. Voltage limit provided by HLMC engineer at GRC.	Test	HiPC.2.2	See HIPC.2
Yoke DISARM Command					
HIPC.2.3	The HiPC shall provide a Disarm signal to the HLMCs when both of the conditions below are satisfied: 1. The Yoke DISARM switch in the cockpit is engaged AND 2. The ARM/DISARM switch in the cockpit is in the ARM position	A yoke mounted disarm switch will allow the pilot to quickly disarm the HLMC while using only his left thumb. This is the same functionality as flipping the instrumented panel ARM/DISARM switch to the Disarm position.	Demonstration	HIPC.2	See HIPC.2
HIPC.2.3.1	The HiPC Disarm signal from the Yoke Disarm switch in the cockpit shall provide a momentary open circuit for at least 0.010 ms.	The yoke disarm switch is a spring loaded push button switch. The switch is normally closed and will provided momentary open circuit when engaged by the pilot before returning to the normally closed position.	Test	HIPC.2.3	See HIPC.2

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC.2.3.1.1	The HiPC Disarm open circuit from the Yoke Disarm switch in the cockpit shall have a resistance of at least 100k Ω as measured at the Disarm input to the HiPC.	More than 100k Ω of resistance is adequate to indicate an open circuit.	Test	HIPC.2.3.1	See HIPC.2
HIPC.2.3.2	The HiPC shall continue to assert the Disarm signal initiated by the Yoke Disarm switch to the HLMCs until a reset is issued by the instrument panel ARM/DISARM switch.	The yoke mounted disarm switch is intended to quickly Disarm the HLMC, and latch the Disarm signal, until a reset is initiated by the ARM/DISARM switch.	Test	HIPC.2.3	See HIPC.2
HIPC.2.3.2.1	The HiPC shall issue a Disarm Reset when the cockpit ARM/DISARM switch is placed to the DISARM position.	This resets the Yoke disarm command and allows for the pilot to resume normal HLMC operations.	Test	HIPC.2.3.2	See HIPC.2
HIPC.2.3.2.2	The HiPC system shall detect when the Yoke Disarm switch has opened the Arm circuit but the instrument panel ARM/DISARM switch is still in the ARM position.	The HiPC needs to detect a switch mismatch to indicate the mismatch switch status to the cockpit. The expected response in the cockpit is defined in requirement HIPC.6.5.	Test	HIPC.2.3.2	See HIPC.2
Airspeed Mode					
HIPC.3	The HiPC shall provide an Airspeed Mode signal to the HLMCs when the AIRSPEED/FIXED switch in the cockpit is placed in the AIRSPEED position.	A pilot selectable switch is used to place the HLMC in an Airspeed Mode or a Fixed Mode. In the Airspeed Mode, the HLMC commands a motor RPM based on an airspeed schedule. In the Fixed Mode, the HLMC commands a fixed motor RPM of 4800 RPM.	Demonstration	C.6.1.3	HR-30.1 Cause C Mit 15 HR-30Cause I, K Mit 15
HIPC.3.1	The HiPC Airspeed mode signal from the AIRSPEED/FIXED switch in the cockpit shall be a closed circuit.	A closed circuit will prevent the HLMC accidently going into the airspeed mode due to open circuit caused by a broken wire or unmated connector. Fixed Mode is the failsafe condition for the HLMC.	Test	HiPC.3	See HIPC.3

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC.3.1.1	The HiPC Airspeed mode closed circuit from the AIRSPEED/FIXED switch in the cockpit shall have a resistance of less than 10 Ω as measured at the Airspeed input to the HiPC.	10 Ω of resistance is adequate resistance to indicate a closed circuit. This would include wire resistance, connector resistance switch closure resistance plus margin.	Test	HIPC.3.1	See HIPC.3
HIPC.3.2	The HiPC Airspeed Mode voltage output signal provided to the HLMC shall reference the HiPC power return	The LCA715STR opto-isolator in the HLMC is a single ended device and does not accept a differential signal.	Test	HIPC.3	See HIPC.3
HIPC.3.2.1	The HiPC Airspeed Mode voltage output signal provided to the HLMC shall range between 14 VDC to 16 VDC	A voltage must be applied to the HLMC input to place the motors in the Airspeed Mode. This will prevent the HLMC from defaulting to the airspeed mode due to a loss of voltage. The HLMC has 630 ohms in series with the LCA715STR opto-isolator LED to activate the Airspeed Mode command. 14 VDC will continually source 20.3ma into the LED. 16 VDC will continually source 23.5ma. The minimum current required to activate the opto-isolator LED is 1ma to 5ma. Peak current is 50ma continuous or 1amp for 10ms. 20 to 25ma will provided a robust signal to activate the LED for the Airspeed Mode command.	Test	HIPC.3.2	See HIPC.3
HIPC.3.2.1.1	The HIPC Airspeed Mode signal shall have a current limit of 30 ma	The output current must below the peak input current for the LCA715STR opto-isolator LED.	Test	HIPC.3.2.1	See HIPC.3

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
Fixed Mode					
HIPC.4	The HiPC shall provide a Fixed Mode signal to the HLMCs when the AIRSPEED/FIXED switch in the cockpit is placed in the FIXED position.	A pilot selectable switch is used to place the HLMC in an Airspeed Mode or a Fixed Mode. In the Airspeed Mode, the HLMC commands a motor RPM based on an airspeed schedule. In the Fixed Mode, the HLMC commands a fixed motor RPM of 4800 RPM.	Demonstration	C.6.1.3	HR-30.1 Cause C Mit 15 HR-30 Cause I, K Mit 15
HIPC.4.1	The HiPC Fixed Mode signal from the AIRSPEED/FIXED switch in the cockpit shall be an open circuit.	The default condition for the HLMC is Disarm. An open circuit caused by a broken wire or an unmated connector will default the HLMC to the Disarm. This is a “fail safe” condition.	Test	HIPC.4	See HIPC.4
HIPC.4.1.1	The HiPC Fixed Mode open circuit from the AIRSPEED/FIXED switch in the cockpit shall have a resistance of at least 100k Ω as measured at the Arm input to the HiPC.	More than 100k Ω of resistance is adequate to indicate an open circuit.	Test	HIPC.4.1	See HIPC.4
HIPC.4.2	The HiPC Fixed Mode signal provided to the HLMC shall be a voltage referenced to the HiPC power return.	The LCA715STR opto-isolator in the HLMC is a single ended device and does not accept a differential signal.	Test	HiPC.4	See HIPC.4
HIPC.4.2.1	The HiPC Fixed Mode signal voltage to the HLMC shall be less than 1.6 VDC.	0 VDC will replicate an open wire or loss of voltage and will cause the HLMC to disarm. This is a “fail safe” condition. Voltage limit provided by HLMC engineer at GRC.	Test	HiPC.4.2	See HIPC.4

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
A/B Architecture					
HIPC.5	The HiPC shall conform to the A/B system architecture define in **Figure 2**.	The A and B high lift propulsors are distributed across the left and right wing so that a failure of an A system or a B system will not produce an abrupt asymmetric thrust event and cause an adverse yaw condition for the aircraft. See **Figure 1** for the high lift propulsors distribution on the wing.	Inspection	V26.1 P24.2	HR-30 Cause C, I and L Mit 4
HIPC.5.1	HiPC-A shall provide command signals to HLMCs at locations 1, 3, 5, 8, 10, and 12.	A failure of HiPC-A system or HiPC-B will not produce an abrupt asymmetric thrust event and cause an adverse yaw condition for the aircraft.	Demonstration	HIPI.5	See HIPC.5
HIPC.5.2	HiPC-B shall provide command signals to HLMCs at locations 2, 4, 6, 7, 9, and 11.	A failure of HiPC-A system or HiPC-B will not produce an abrupt asymmetric thrust event and cause an adverse yaw condition for the aircraft.	Demonstration	HIPI.5	See HIPC.5

6.2 HiPC Cockpit Requirements

These requirements apply to the cockpit switches and indicators that interface to the HiPC-A and HiPC-B. Please refer to **Figure 2** for the cockpit interface boundaries

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HiPC					
HIPC.6	The HiPC switches and indicators shall follow the layout configuration as defined in the Cockpit ICD (ICD-CEPT-006).	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	V5.2	HR30
HIPC.6.1	The HiPI switches and indicator labeling shall meet the requirements defined in MIL-STD-1472H, section 5.4.2 through 5.4.3.	MIL-STD-1472H dictates this as a Human Systems Integration Requirement.	Inspection	HIPC.6	See HIPI.6
HIPC.6.2	The HIPC Yoke Disarm switch shall reside on the cockpit yoke.	A yoke switch allows for quick Disarming of the HL system.	Inspection	C3.1.4	HR-30.2 Mit. 8 HR-30.1 Mit. 13, HR-30 Cause H, J, Mit. 13
HIPC.6.2.1	The HiPC Yoke Disarm switch shall use a momentary style of switch.	A momentary switch is located on the Yoke to quickly disarm the system.	Inspection	HIPC.6.2	See HIPC.6.2
HIPC.6.3	The HIPC ARM/DISARM switch shall reside on the instrument panel.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	C3.1.1 C3.1.4	See HIPC.6.2
HIPC.6.3.1	The HIPC ARM/DISARM switch shall ARM and DISARM the high lift system.	A switch is needed to close or open the Arm circuit.	Inspection	HIPC.6.3	See HIPC.6.2
HIPC.6.4	The HIPC Mode Control select switch shall reside on the instrument panel.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	V3.1.7 V6.1	See HIPC.6.2

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC.6.4.1	The HIPC Mode Select switch shall select Fixed or Airspeed mode operations.	The HL system has two modes of control, Fixed and Airspeed.	Inspection	HIPC.6.4	HR-30.1 Cause C Mit 15 HR-30.2 Cause I, K Mit 15
HIPC.6.5	The HiPC system shall send an electrical output to the Reset Required indicator when a switch mismatch is detected as described in Requirement HIPC.2.3.2.2.	Quickly alerts the pilot the Yoke Disarm switch was engaged to Disarm the HL system instead of the Arm/Disarm Switch.	Test	C3.1.4 P.26.1.1	See HIPC.6.2
HIPC.6.5.1	The HiPC system Reset Required indicator shall reside on the instrument panel.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	HIPI.6.3	See HIPC.6.2
HIPC.6.5.2	The HiPC Reset Required indicator shall be sunlight-readable in accordance with luminance criteria in MIL-STD-1472H, 5.2.3.3.3.1 through 5.2.3.3.3.4.	Ensures indicators are readable in the flight environment.	Demonstration	HIPI.6.5	See HIPC.6.2
HiPC.6.5.3	The HiPC shall receive a signal from the X-57 Cockpit Light Check switch to illuminate the HiPC Reset Required indicator.	One switch in the cockpit verifies all cockpit indicators turn on and illuminate. This is performed as part of a preflight test.	Demonstration	HIPI.6.5	See HIPC.6.2
HiPC.6.5.3.1	The HiPC signal received from the X-57 Cockpit Light Check switch shall be a closed circuit.	The X-57 Cockpit Light Check switch is a “Push to Test” switch is normally open and closes when engaged by the pilot.	Demonstration	HIPI.6.5.3	See HIPC.6.2
HiPC.6.5.3.2	The HiPC closed circuit resistance received from X-57 Cockpit Light Check switch shall be less than 10 Ω as measured at the input to the HiPC.	10 Ω of resistance is adequate resistance to indicate a closed circuit. This would include wire resistance, connector resistance switch closure resistance plus margin.	Test	HIPI.6.5.3	See HIPC.6.2

7 High Lift Propeller Indicator (HiPI) Requirements

7.1 HiPI Interface Requirements

These requirements apply to HiPI-A and HiPI-B. Please refer to **Figure 2** for the HiPI-A and HiPI-B interface boundaries

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HiPI Cockpit Interface					
HIPI.1	The HiPI shall report the status of the HLMC to the cockpit.	The HiPI is the interface between the HLMCs and the cockpit status indicators for the High Lift System.	Inspection	C.2.3.3	HR-30 Cause A, C, H, I, K Mit. 6
HIPI.1.1	The HiPI shall provide electrical outputs to illuminate the Pilot Cockpit Status Indicators.	The Pilot Indicators will provide the HL system status during flight operations.	Inspection	HIPI.1	See HIPI.1
HIPI.1.1.1	The HiPI shall illuminate the Pilot Cockpit Status Indicators as defined in **Table 1**.	The Cockpit Pilot Indicators report a combined status for the HL system status based on the status of multiple HLMCs. The display is simple so the pilot can quickly asses the status of the high lift system.	Test	HIPI.1.1	See HIPI.1
HIPI.1.1.2	The HiPI shall illuminate the Pilot Cockpit Status Indicators based on the priority logic defined in **Table 1**.	To simplify the amount of information available to the Pilot, a priority must be assigned to each indicator.	Test	HIPI.1.1	See HIPI.1
HIPI.1.2	The HiPI shall provide electrical outputs to illuminate the Cockpit Ground Crew Indicators.	The Ground Crew Cockpit Status Indicators will provide the HL system status during ground operations, including system testing.	Inspection	HIPI.1	See HIPI.1
HIPI.1.2.1	The HiPI system shall illuminate the Ground Crew Cockpit Status Indicators as defined in **Table 2**.	The Ground Crew Cockpit Status Indicators reports the status of each HLMC. This will allow the ground crew quickly identify the status of each HLMC.	Test	HIPI.1.2	See HIPI.1

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HiPI HLMC Interface					
HIPI.2	The HiPI shall receive four HLMC discrete status signals from each HLMC.	The four discrete signal will provide the status for each HLMC.	Inspection	C2.3.3	HR30 Cause A, C, H, I, K Mit. 6
HIPI.2.1	The HiPI discrete status signal received from the HLMC shall be an open circuit to represent a low level logic state.	An open circuit (off) represents a Logic Level 0.	Test	HIPI.2	See HIPI.2
HIPI.2.1.1	The HiPI discrete status signal open circuit resistance received from the HLMC shall be at least 100k Ω as measured at the input to the HiPI.	More than 100k Ω of resistance is adequate to indicate an open circuit.	Test	HIPI.2	See HIPI.2
HIPI.2.2	The HiPI discrete status signal received from the HLMC shall be a closed circuit to represent a high level logic state.	A closed circuit (on) represents a Logic Level 1.	Test	HIPI.2	See HIPI.2
HIPI.2.2.1	The HiPI discrete status signal closed circuit resistance received from the HLMC shall be less than 10 Ω as measured at the input to the HiPI.	10 Ω of resistance is adequate resistance to indicate a closed circuit. This would include wire resistance, connector resistance switch closure resistance plus margin.	Test	HIPI.2	See HIPI.2
HIPI.2.3	The HiPI discrete status signals shall be labeled GPIO 10, GPIO 11, GPIO 12 and GPIO 13.	Provides HLMC signal labels for cockpit displays logic table.	Inspection	HIPI.2	See HIPI.2
HIPI.2.4	The HiPI system shall electrically isolate the HLMC GPIO signals from the HiPC signal conditioning.	Signal isolation is required to preserve signal integrity.	Test	C.1.1.3	HR-19B Cause C, Mit. 4
A/B Architecture					
HIPI.3	The HiPI system shall consist of two identical, independent systems labeled Side A and Side B.	The HiPI architecture should match existing aircraft architectures.	Inspection	V26.1 P24.2	HR-30 Cause C, I and L Mit. 4
HIPI.3.1	HiPI-A shall process status signals from HLMCs at locations 1, 3, 5, 8, 10, and 12.	Side A of other vehicle systems, such as avionics and traction power distribution systems, is defined as listed.	Demonstration	HIPI.3	See HIPI.3

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPI.3.2	HiPI-B shall process status signals from HLMCs at locations 2, 4, 6, 7, 9, and 11.	Side B of other vehicle systems, such as avionics and traction power distribution systems, is defined as listed.	Demonstration	HIPI.3	See HIPI.3
HIPI.3.3	The HiPI electrical output shall use discrete logic.	Simple architectures should be used where possible. Simplifies control and design validation.	Inspection	HIPI.3	See HIPI.3

Table 1 – Pilot Cockpit Status Indicators

○ Indicator Off, ● Indicator On, ◑ Indicator Flashing

Priority	Rule	HLMC GPIO (10-11-12-13)	Status
Indicator 1			
1	If all 'Ready'	0-1-0-0	●
2	If all 'Airspeed Run'	1-0-0-1	●
3	If any 'Maintenance'	1-1-0-1 1-1-1-0 1-1-1-1	●
4	If any 'Init'	0-0-0-1	◑
5	If any 'Waiting'	0-0-1-1	◑
6	If any 'Airspeed Default Run'	1-0-1-0	◑
7	If any 'Ready'	0-1-0-0	◑
8	If any 'Airspeed Run'	1-0-0-1	◑
9	Else		○
Indicator 2			
1	If all 'Fixed Run'	1-0-0-0	●
2	If all 'Airspeed Run'	1-0-0-1	●
3	If any 'Maintenance'	1-1-0-1 1-1-1-0 1-1-1-1	●
4	If any 'Spin Up'	0-1-1-1	◑
5	If any 'Spin Down'	0-1-1-1	◑
6	If any 'Airspeed Default Run'	1-0-0-1	◑
7	If any 'Fixed Run'	1-0-0-0	◑
8	If any 'Airspeed Run'	1-0-0-1	◑
9	Else		○
Indicator 3			
1	If any 'Maintenance'	1-1-0-1 1-1-1-0 1-1-1-1	●
2	If any 'Armed Fault'	1-0-1-1	◑
3	If any 'HV Fault'	0-1-1-0	●
4	If any 'Air Data Fault'	0-1-0-1	●
5	If any 'Terminal Fault'	1-1-0-0	●
6	If any 'PUBiT Fault'	0-0-1-0	●
7	Else		○

Table 2 – Ground Crew Cockpit Status Indicators

○ Indicator Off, ● Indicator On, ◑ Indicator Flashing

Ground Crew Cockpit Indicators		
HLMC GPIO 10-11-12-13	**Ground Crew Indicator (x12)**	**HLMC Condition**
0-0-0-0	○ ○ ○	Off
0-0-0-1	◑ ◑ ◑	Initializing
0-0-1-0	◑ ◑ ●	PUBiT Fault
0-0-1-1	◑ ○ ○	Waiting
0-1-0-0	● ○ ○	Ready
0-1-0-1	◑ ○ ●	Air Data Fault
0-1-1-0	◑ ○ ●	HV Fault
0-1-1-1	○ ◑ ○	Spin Up Spin Down Maintenance - Test
1-0-0-0	○ ● ○	Fixed Run
1-0-0-1	● ● ○	Airspeed Run
1-0-1-0	◑ ◑ ○	Airspeed Default Run
1-0-1-1	○ ○ ◑	Armed Fault
1-1-0-0	○ ○ ●	Terminal Fault
1-1-0-1	● ◑ ◑	Maintenance - Load
1-1-1-0	◑ ○ ◑	Maintenance - Ready
1-1-1-1	○ ◑ ●	Maintenance - Fault

7.2 HiPI Cockpit Status Indicator Requirements

These requirements apply to the cockpit indicators that interface to the HiPI-A and HiPI-B. Please refer to **Figure 2** for the cockpit interface boundaries

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPI.5	The HIPI system cockpit status indicators shall reside on the cockpit instrument panel.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	V5.2 C2.3.3	HR30 Cause A, C, H, I, K Mit. 6
HIPI.5.1	The HiPI cockpit status indicator's flash rate shall be no greater than 5 Hz and no less than 0.8 Hz.	MIL-STD-1472H 5.17.27.3.3 dictates this as a Human Systems Integration Requirement.	Demonstration	HIPI.5	See HIPI.5
HIPI.5.1.1	The HiPI cockpit status indicator's flash rate duty cycle percentage of "on" time shall be equal to but not less than the percentage of "off" time.	MIL-STD-1472H 5.17.27.2 dictates this as a Human Systems Integration Requirement. A 50 percent duty cycle is preferred.	Demonstration	HIPI.5.1	See HIPI.5
HIPI.5.2	The HiPI flashing cockpit status indicator's ~~flash~~ shall be synchronized.	FAA AC 25.1322-1 dictates this as Human Systems Integration Requirement.	Demonstration	HIPI.5	See HIPI.5
HIPI.5.3	The HiPI cockpit status indicators shall be sunlight-readable in accordance with luminance criteria in MIL-STD-1472H, 5.2.3.3.3.1 through 5.2.3.3.3.4.	Ensures indicators are readable in the flight environment.	Demonstration	HIPI.5	See HIPI.5
HIPI.5.4	The HiPI Ground Crew Cockpit Status Indicators shall reside on the instrument panel.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	HiPI.5	See HIPI.5
HIPI.5.4.1	HIPI-A shall illuminate status indicators on the Ground Crew Cockpit Status Indicator display for HLMCs 1, 3, 5, 8, 10, 12.	The Ground Crew Cockpit Indicator displays the status for all A bus HLMCs (See Table 2, Cockpit Ground Crew Cockpit Status Indicator).	Demonstration	HIPI.5.4	See HIPI.5
HIPI.5.4.1.1	HIPI-A shall illuminate 3 status indicators on the Ground Crew Cockpit Status Indicator for each HLMC.	HIPI-A encompasses six HLMCs. Each HLMC has three status indicators (blue, green, red) for a total of 18 indicators.	Demonstration	HIPI.5.4.1	See HIPI.5

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPI.5.4.2	HIPI-B shall illuminate status indicators on the Ground Crew Cockpit Status Indicator display for HLMCs 2, 4, 6, 7, 9, 11.	The Ground Crew Cockpit Status Indicator displays the status for all B bus HLMCs (See Table 2, Ground Crew Cockpit Status Indicator).	Demonstration	HIPI.5.4	See HIPI.5
HIPI.5.4.2.1	HIPI-B shall illuminate 3 status indicators on the Ground Crew Cockpit Status Indicator for each HLMC.	HIPI-B encompasses six HLMCs. Each HLMC has three status indicators (blue, green, red) for a total of 18 indicators.	Demonstration	HIPI.5.4.2	See HIPI.5
HIPI.5.4.3	The HiPI Ground Crew Cockpit Status Indicators shall follow the layout configuration as defined in the Cockpit ICD (ICD-CEPT-006) Rev B Page 56.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	HIPI.5	See HIPI.5
HIPI.5.4.3.1	The HiPI Ground Crew Cockpit Status Indicator labeling shall meet the requirements defined in MIL-STD-1472H, section 5.4.2 through 5.4.3.	MIL-STD-1472H dictates this as a Human Systems Integration Requirement.	Inspection	HIPI.5.4.3	See HIPI.5
HIPI.5.5	The HiPI Pilot Cockpit Status Indicators shall reside on the instrument panel.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	HIPI.5	See HIPI.5
HIPI.5.5.1	HIPI-A shall illuminate three status indicators on the Pilot Cockpit Status Indicators for HLMCs 1, 3, 5, 8, 10 and 12.	HiPI-A will process a combined output from 6 HLMCs to drive three status indicators for the Pilot. (See Table 1, Pilot Cockpit Status Indicators).	Demonstration	HIPI.5.5	See HIPI.5
HIPI.5.5.2	HIPI-B shall illuminate three status indicator on the Pilot Cockpit Status Indicators for HLMCs 2, 4, 6, 7, 9 and 11.	HiPI-B will process a combined output from 6 HLMCs to drive three status indicators for the Pilot. (See Table 1, Pilot Cockpit Status Indicators).	Demonstration	HIPI.5.5	See HIPI.5
HIPI.5.5.3	The HiPI Pilot Cockpit Status Indicators shall follow the layout configuration as defined in the Cockpit ICD (ICD-CEPT-006) Rev B Page 56.	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006). Required to be in the pilot's field of view.	Inspection	HIPI.5.5	See HIPI.5

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPI.5.5.3.1	The HiPI Pilot Cockpit Status Indicator labeling shall meet the requirements defined in MIL-STD-1472H, section 5.4.2 through 5.4.3.	MIL-STD-1472H dictates this as a Human Systems Integration Requirement.	Inspection	HIPI.5.5.3	See HIPI.5
HIPI.5.6	The HiPI cockpit status indicators panels shall fit in designated areas as defined in the Cockpit ICD (ICD-CEPT-006).	The cockpit layout is defined in the Cockpit ICD (ICD-CEPT-006).	Inspection	HIPI.5	See HIPI.5
HiPI.5.7	The HiPI shall receive a signal from the X-57 Cockpit Light Check switch to illuminate the HiPI cockpit status indicators.	One switch in the cockpit verifies all cockpit indicators turn on and illuminate. This is performed as part of a preflight test.	Demonstration	HIPI.5	See HIPI.5
HiPI.5.7.1	The HiPI signal received from the X-57 Cockpit Light Check switch shall be a closed circuit.	The X-57 Cockpit Light Check switch is a “Push to Test” switch is normally open and closes when engaged by the pilot.	Demonstration	HIPI.5.7	See HIPI.5
HiPI.5.7.2	The HiPI closed circuit resistance received from X-57 Cockpit Light Check switch shall be less than 10 Ω as measured at the input to the HiPI.	10 Ω of resistance is adequate resistance to indicate a closed circuit. This would include wire resistance, connector resistance switch closure resistance plus margin.	Test	HIPI.5.7	See HIPI.5

8 HiPI and HiPC Combined Requirements

These requirements apply to HiPC-A, HiPC-B, HiPI-A and HiPI-B. Please refer to **Figure 2** for the HiPC-A, HiPC-B HiPI-A and HiPI-B interface boundaries

8.1 Power Requirements

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC_HIPI.1	The HiPC and HiPI system shall receive power from the aircraft Essential Bus.	The essential bus is used to power essential circuits.	Inspection	V.13.1.1 P.13.1	HR-14 Cause B Mit 2
HIPC_HIPI.1.1	The HiPC and HiPI system shall operate over an input voltage range of 11.5 to 32VDC.	We plan to power the HiPI from a 24 VDC power supply that receives its power form the Aircraft 13.8 VDC essential bus. This design is still preliminary. The 11.5 VDC to 32 VDC range provides options to power the system with 13.8 VDC, 24 VDC or 28 VDC.	Test	HIPC_HIPI.1	See HIPC_HIPI.1
HIPC_HIPI.1.2	The HiPC and HiPI total power consumption shall be less than 40 watts.	The HiPI and HiPC are allocated 40 watts of essential bus power. Power required during the momentary preflight Light Check defined in HiPC.6.5.3 and HiPI.5.7 can exceed this 40 watt allocation.	Test	HIPC_HIPI.1	See HIPC_HIPI.1
HIPC_HIPI.1.3	The HiPC power shall be electrically isolated from the HiPI power.	For reliability, the HiPC and HiPI are independently powered, and signals isolated. Each system will have independent breakers in the cockpit as showed in Figure 2.	Test	HIPC_HIPI.1	See HIPC_HIPI.1
HIPC_HIPI.1.3.1	The HiPC-A power shall be electrically isolated from the HiPC-B power.	For reliability, the HiPC-A and HiPC-B are independently powered, and signals isolated.	Test	HIPC_HIPI.1	See HIPC_HIPI.1

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
		Each system will have independent breakers in the cockpit as showed in Figure 2.			
HIPC_HIPI.1.3.2	The HiPI-A power shall be electrically isolated from the HiPI-B power.	For reliability, the HiPI-A and HiPI-B are independently powered, and signals isolated. Each system will have independent breakers in the cockpit as showed in Figure 2.	Test	HIPC_HIPI.1	See HIPC_HIPI.1

8.2 Weight Requirements

Req. #	Requirement	Rationale	Verification Method	Requirements Trace	Safety Critical
HIPC_HIPI.2	The HiPC and HiPI system weight shall be less than 4.2 lbs.	This includes HiPI-A, HiPI-B, HiPC-A, HiPC-B, the Airspeed/Fixed Mode Cockpit Switch panel, the Arm/Disarm Cockpit Switch panel, the Pilot Indicators panel, Ground Crew indicator panel and Yoke Disarm switch. It does not include interface cables or the connectors on the interface cables.	Test	V.3.1.2	HR-20B Cause C, Mit. E

8.3 Environmental Test Requirements

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.3	The HiPI and HiPC system shall meet NASA standards defined for Zone 2 (Cabin) in X57 Environmental Test Plan, ETP-CEPT-007.	Verify system will function as designed in the flight environment.	Test	SRD 30	HR-30 Mit 1

8.4 Structural Requirements

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.4	The HiPC and HiPI system enclosure structures shall meet the structural loads requirements in REQ-CEPT-007," SCEPTOR Structural Loads Requirements for Floor and Equipment Support".	Verifies HiPI mounting structure will meet crash loads requirements.	Analysis	SRD 32	No

8.5 Fabrication Requirements

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.5	The HiPC and HiPI system shall meet the Armstrong Flight Research Center workmanship standards.	Ensures HIPI/HIPC will meet AFRC workmanship standards as stated in QAP-CEPT-008 Section 6.2.1.	Inspection	SRD 31	HR-30 Mit 3

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.5.1	The HiPC and HiPI system shall comply with IPC/WHMA-A-620B workmanship standard for the manufacture of cable, wire and harness assemblies.	Ensures HIPI/HIPC wire and harness assemblies will meet AFRC workmanship standards as stated in QAP-CEPT-008 Section 6.2.1.	Inspection	HIPC_HIPI.5	See HIPC_HIPI.5
HIPC_HIPI.5.2	The HiPC and HiPI system shall comply with the IPC J-STD-001 workmanship standard for soldered electrical and electronic assemblies.	Ensures HIPI/HIPC soldering will meet AFRC workmanship standards as stated in QAP-CEPT-008 Section 6.2.1.	Inspection	HIPC_HIPI.5	See HIPC_HIPI.5
HIPC_HIPI.5.3	The HiPC and HiPI Printed circuit board (PCB) shall comply with IPC-6012 Class 2.	Ensures HIPI/HIPC PCBs will meet AFRC workmanship standards as stated in QAP-CEPT-008 Section 6.2.1.	Inspection	HIPC_HIPI.5	See HIPC_HIPI.5
HIPC_HIPI.5.4	The HiPC and HiPI system and other multi-conductor assemblies shall consist of basic components listed under Military Specification MIL-C-27500 (uses MIL-DTL-22759) or MIL-W-16878D (uses MIL-W-16878).	Ensures cable assemblies meet AFRC airworthiness standards for flight hardware per QAP-CEPT-008 Appendix A (PQA Q-4).	Inspection	HIPC_HIPI.5	See HIPC_HIPI.5
HIPC_HIPI.5.5	The HiPC and HiPI system shall comply ANSI/ESD S20.20 ESD Control program.	Protect electrical or electronic parts, assemblies, and equipment susceptible to damage by electrostatic discharges greater than or equal to 100 volts HBM, 200 volts CDM, and 35 volts on isolated conductors.	Inspection	HIPC_HIPI.5	See HIPC_HIPI.5

8.6 Derating of Electrical and Electronic Parts Requirements

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.6	The HiPC and HiPI system electrical, electronic and electro-mechanical components shall have a de-rating factor applied.	Provides design margin per the guidance provided in AFOP-8730.2-002 - EEE Parts Management & Control for Electronic Flight Hardware.	Analysis	SRD 31	HR-30 Mit 2
HIPC_HIPI.6.1	The HiPC and HiPI system capacitors de-rating calculations shall use a de-rating to 60% of rated voltage, 70% of rated current.	Provides design margin for capacitors.	Analysis	HIPC_HIPI.6	HR-30 Mit 2
HIPC_HIPI.6.2	The HiPC and HiPI system resistors de-rating calculations shall use a de-rating of 60% of rated power (average).	Provides design margin for resistors.	Analysis	HIPC_HIPI.6	HR-30 Mit 2
HIPC_HIPI.6.3	The HiPC and HiPI system diodes de-rating calculations shall use a de-rating to 70% peak inverse voltage, 50% of rated power, 50% of rated forward current, 40 °C less than maximum rated junction temperature.	Provides design margin for diodes.	Analysis	HIPC_HIPI.6	HR-30 Mit 2

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.6.4	The HiPC and HiPI system transistors de-rating calculations shall use a de-rating to 50% of rated power dissipation, 75% of rated current, 75% of rated voltage, 40 °C less than maximum rated junction temperature.	Provides design margin for transistors.	Analysis	HIPC_HIPI.6	HR-30 Mit 2
HIPC_HIPI.6.5	The HiPC and HiPI system linear microcircuits de-rating calculations shall use de-rating to 85% of maximum supply voltage, 80% of maximum input voltage, but not more than supply voltage, 75% of maximum output current, 75% of maximum open collector/drain output voltage, 90% of maximum short circuit output current, 75% of maximum power dissipation, 40 °C less than maximum rated junction temperature.	Provides design margin for linear microcircuits.	Analysis	HIPC_HIPI.6	HR-30 Mit 2
HIPC_HIPI.6.6	The HiPC and HiPI system voltage regulators de-rating calculations shall use a de-rating to 90% of maximum output short circuit current, 80% of maximum input voltage, 75% of maximum output current, 75% of maximum power dissipation, 40 °C less than maximum rated junction temperature.	Provides design margin Voltage regulators.	Analysis	HIPC_HIPI.6	HR-30 Mit 2

Req. #	Requirement	Rationale	Verification Method	Trace	Safety Critical
HIPC_HIPI.6.7	The HiPC and HiPI system digital microcircuits de-rating calculations shall use a de-rating to 80% of maximum fan-out or output current, ±10% from nominal supply voltage, 80% maximum clock speed, 80% of maximum open collector/drain output voltage, 40 °C less than maximum rated junction temperature.	Provides design margin digital microcircuits.	Analysis	HIPC_HIPI.6	HR-30 Mit 2
HIPC_HIPI.6.8	The HiPC and HiPI system wire and cables shall follow the sizing defined in Aerospace Standard AS50881.	Provides design margin for cables and wires.	Analysis	HIPC_HIPI.6	HR-30 Mit 2