

MEMS Deformable Mirror Development



Iris AO, Inc.

NASA Phase SBIRs: NNX14CG06C, NNX16CD58P

**Michael A. Helmbrecht
Iris AO, Inc.**

**www.irisao.com
michael.helmbrecht@irisao.com
info@irisao.com**

Approved for public release; unlimited distribution

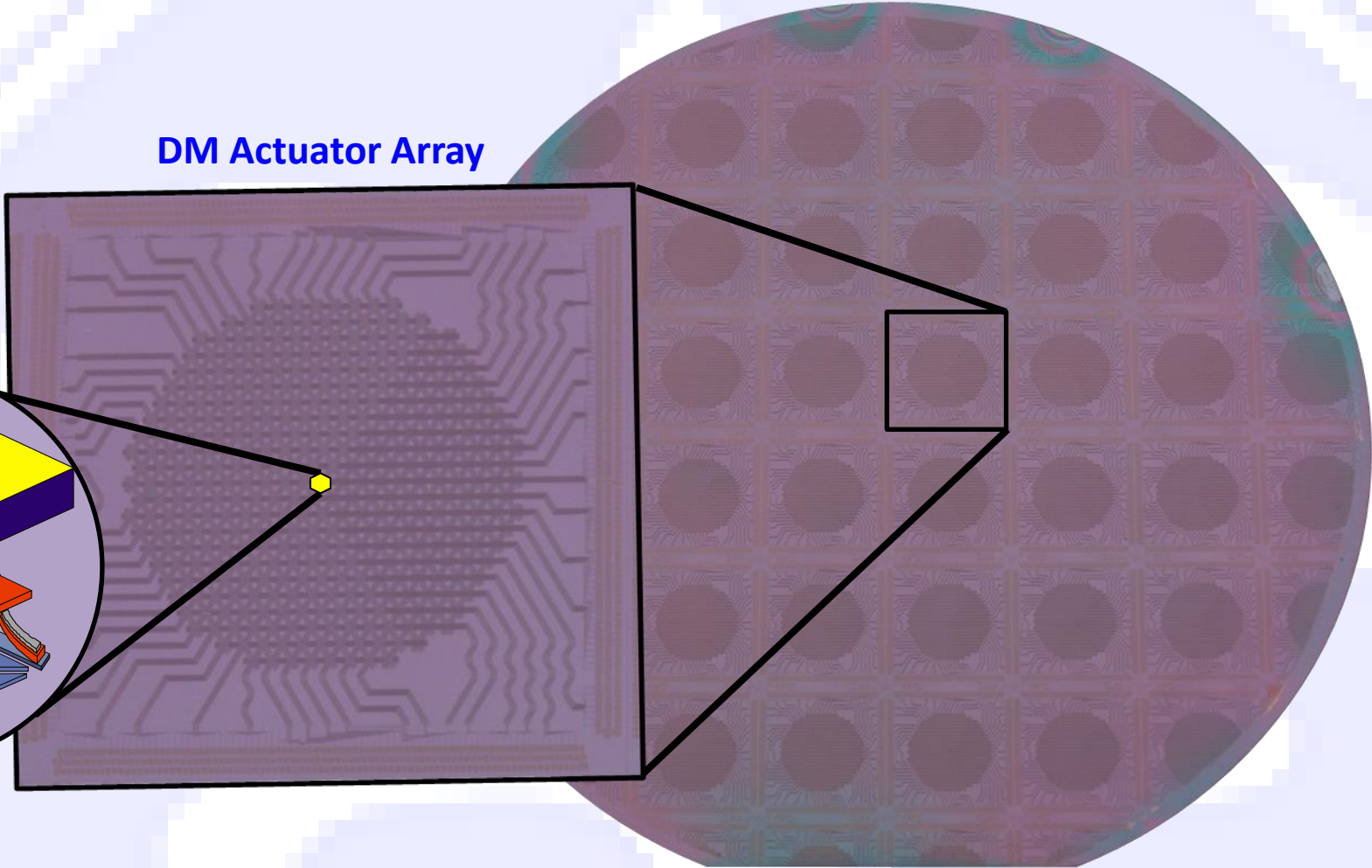
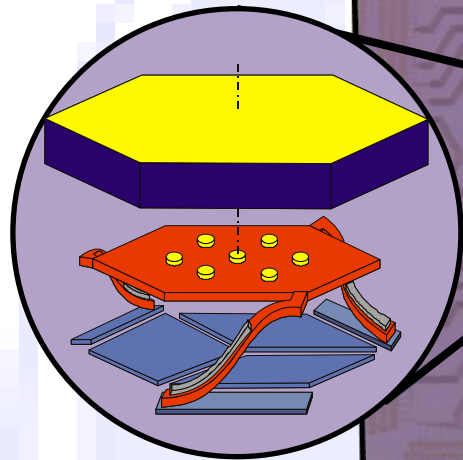
Iris AO Segmented DM Background

Silicon Wafer Processing

DM Actuator Wafer

DM Actuator Array

DM Segment



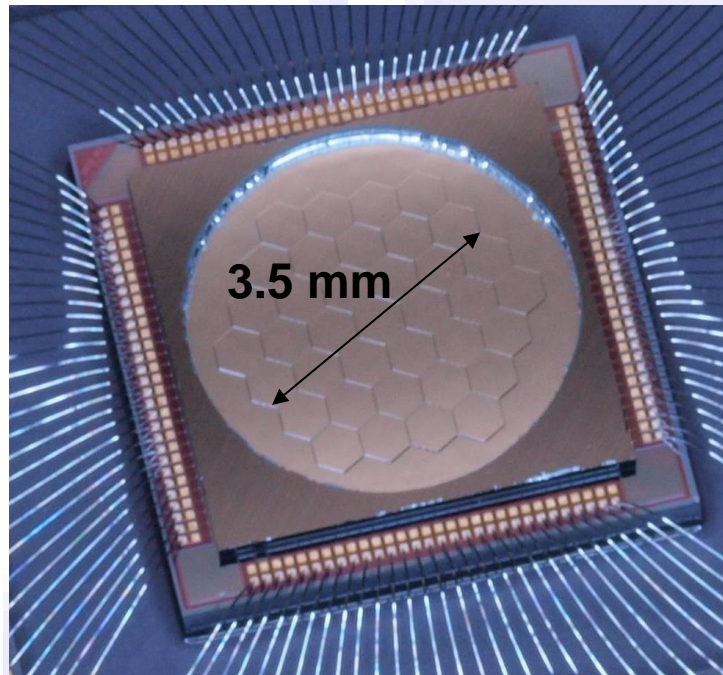
$\Phi=700 \mu\text{m}$

$L=19 \text{ mm}$

$\Phi=150 \text{ mm}$

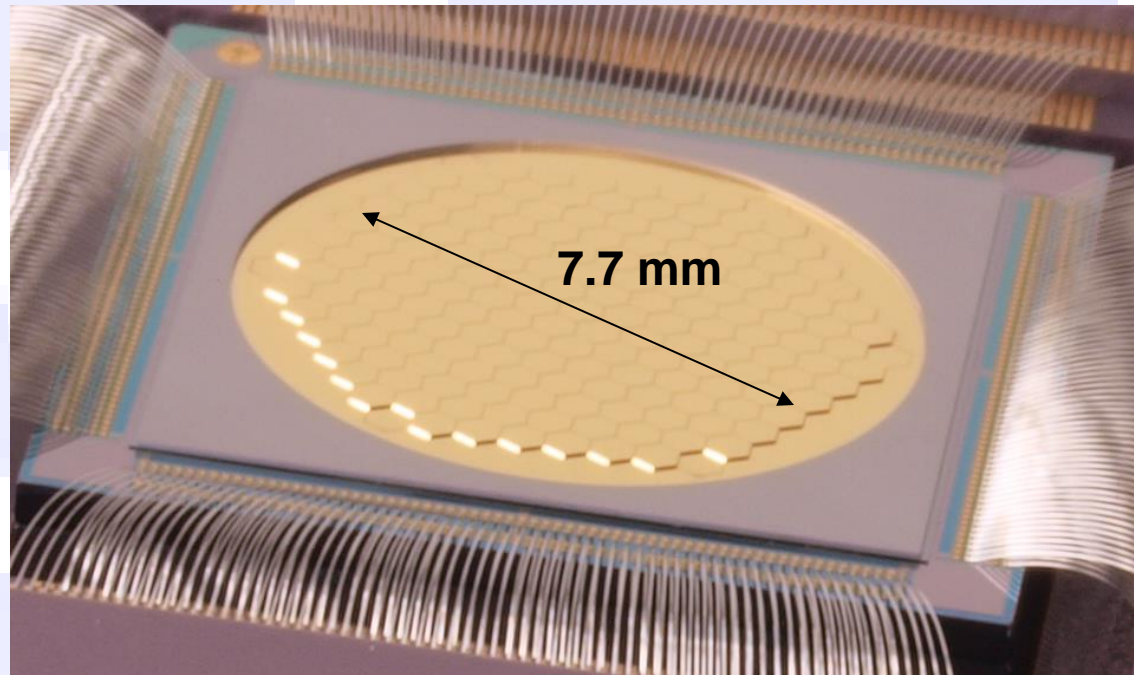


Iris AO MEMS Segmented Deformable Mirrors



PTT111 DM

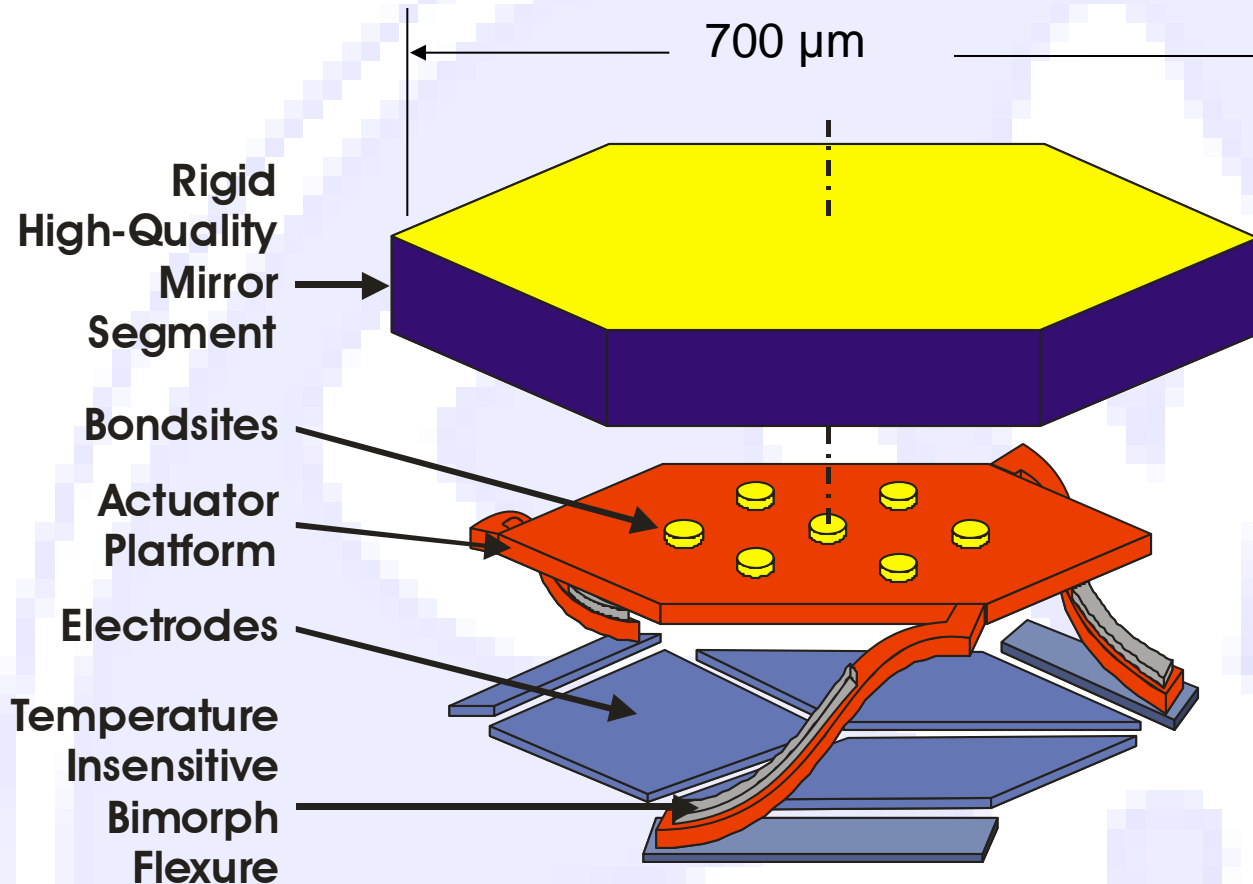
- 111 Actuators
- 37 PTT Segments
- 3.5 mm inscribed aperture
- Factory calibrated



PTT489 DM

- 489 Actuators
- 163 PTT Segments
- 7.7 mm inscribed aperture
- Factory calibrated

Iris AO Segmented DM Background



- **3 DOF: Piston/tip/tilt electrostatic actuation**
 - no hysteresis
- **Hybrid fabrication process**
 - 3-layer polysilicon surface micromachining
 - Single-crystal-silicon assembled mirror
- **Unit cell easily tiled to create large arrays**
- **Hybrid technology**
 - Thick mirror segments
 - $<1 \text{ nm PV}/^\circ\text{C}$ segment bow
 - Enables back-side stress-compensation coatings

DMs calibration holds >30 months, <http://arxiv.org/abs/1609.04742>

Phase II SBIR Development NNX14CG06C

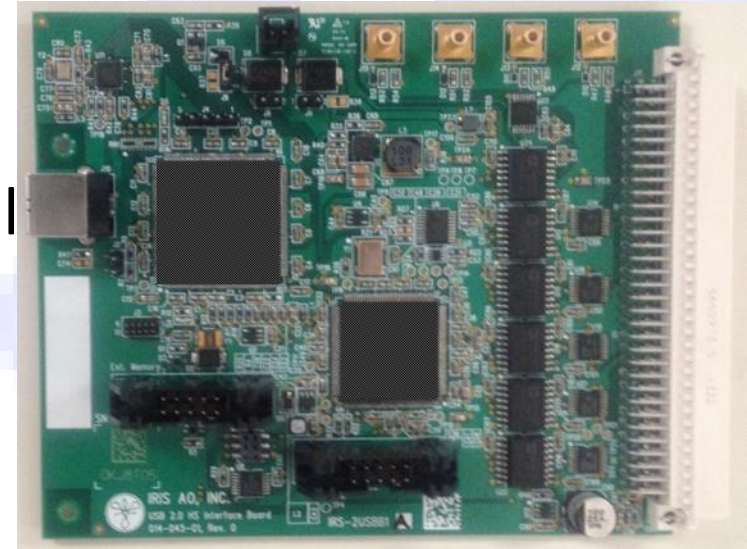
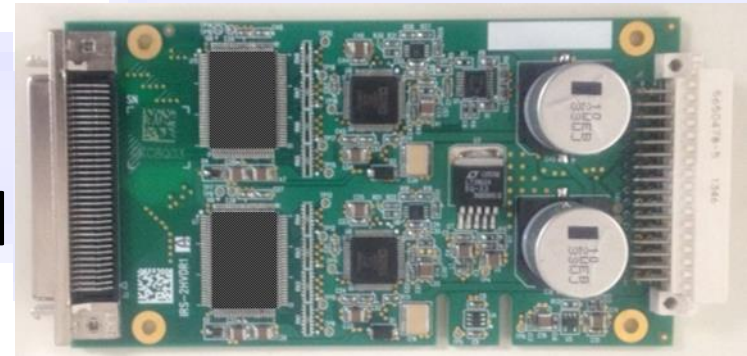
Increasing Phase Resolution

High-Resolution Electronics Development

- Standard Iris AO drive electronics are 14-bit resolution

NNX14CG06C Development

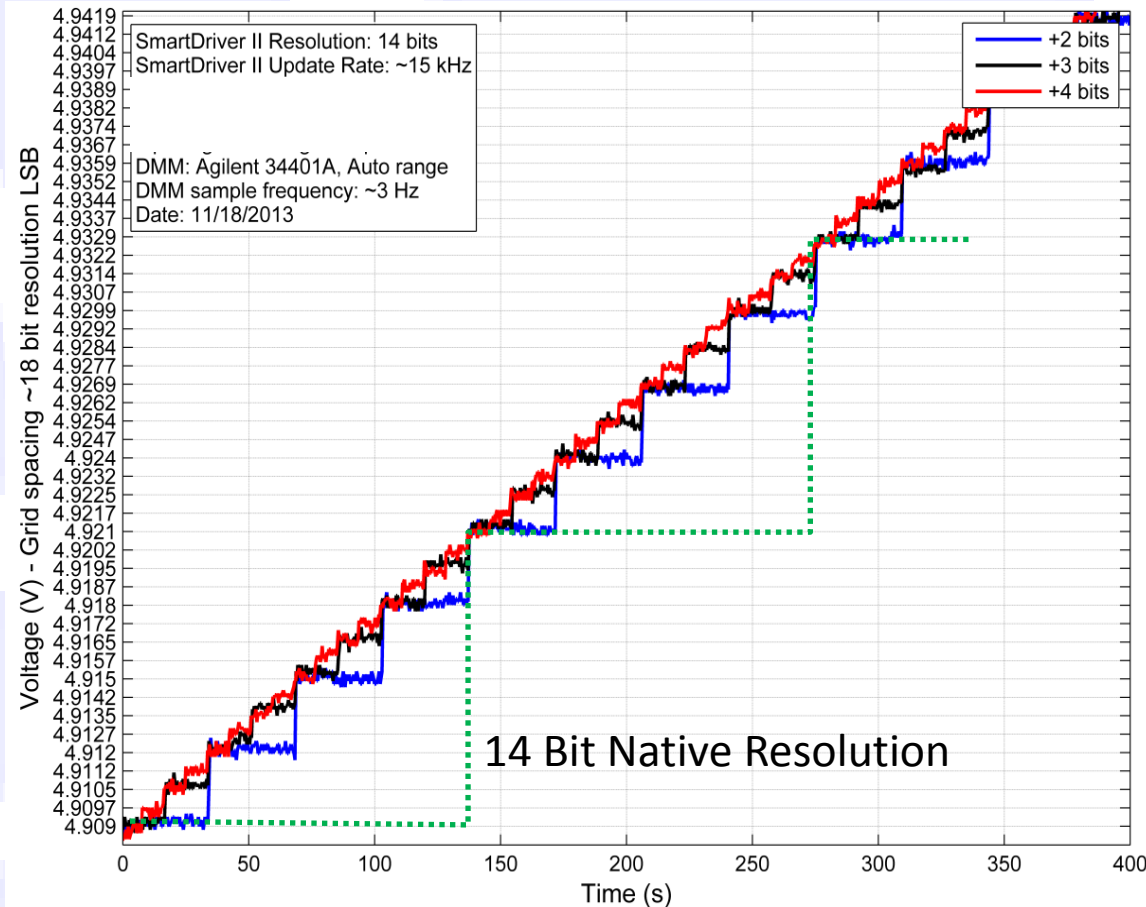
- 16-bit resolution HV driver card
- USB2.0 High-Speed interface
 - Microcontroller
 - FPGA to implement timing critical modulation
 - Windows *and* Linux compatible
 - ~4 kHz updates under Linux



Super-Resolution Drive Electronics

Software-Driven 14-Bit Super-Resolution Results

- Standard electronics are 14 bit (native) resolution
- Super-resolution technique has demonstrated 18-bit resolution
 - Grid spacing is for 1 LSB on 18-bit resolution
 - Software driven control using a PCI interface card
 - Impractical for actual use
- Modulation schemes implemented in FPGA on USB interface card
 - 16 bit – firmware demonstrated
 - 14 bit – firmware under development
- **Expect 20+ bits of resolution**
 - **Limited by electronics noise floor and bandwidth requirements**
- Testing to be complete Q1 2017



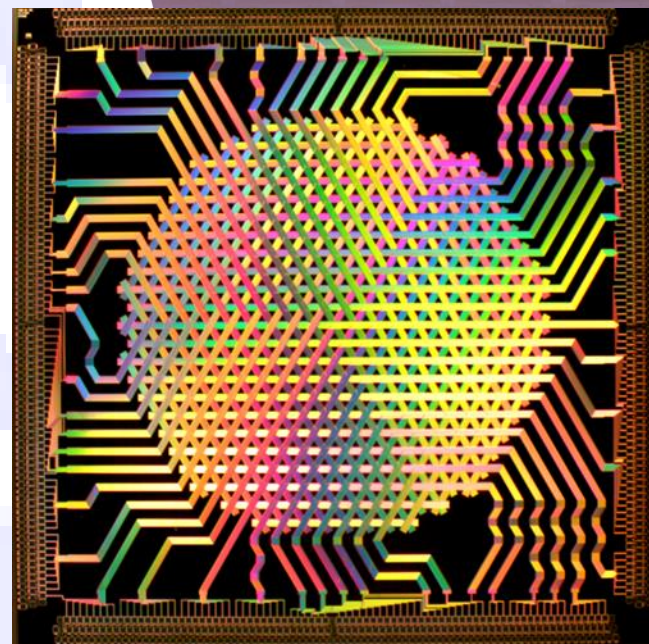
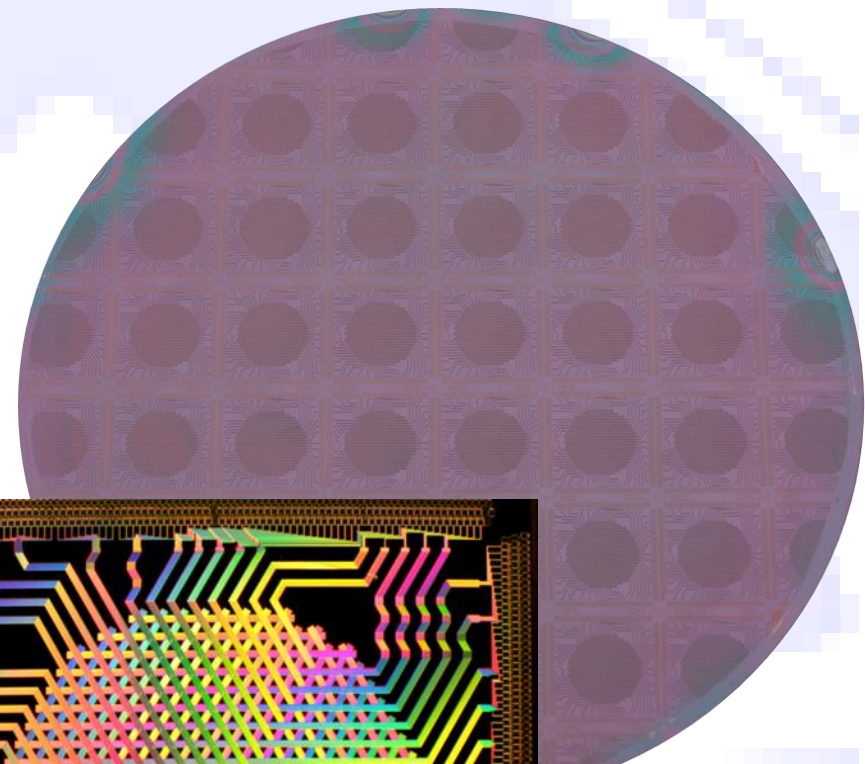
Phase II SBIR Development NNX14CG06C

Increasing Spatial Resolution
(Increasing Yield)



PTT939: 1000-Actuator DM Fabrication

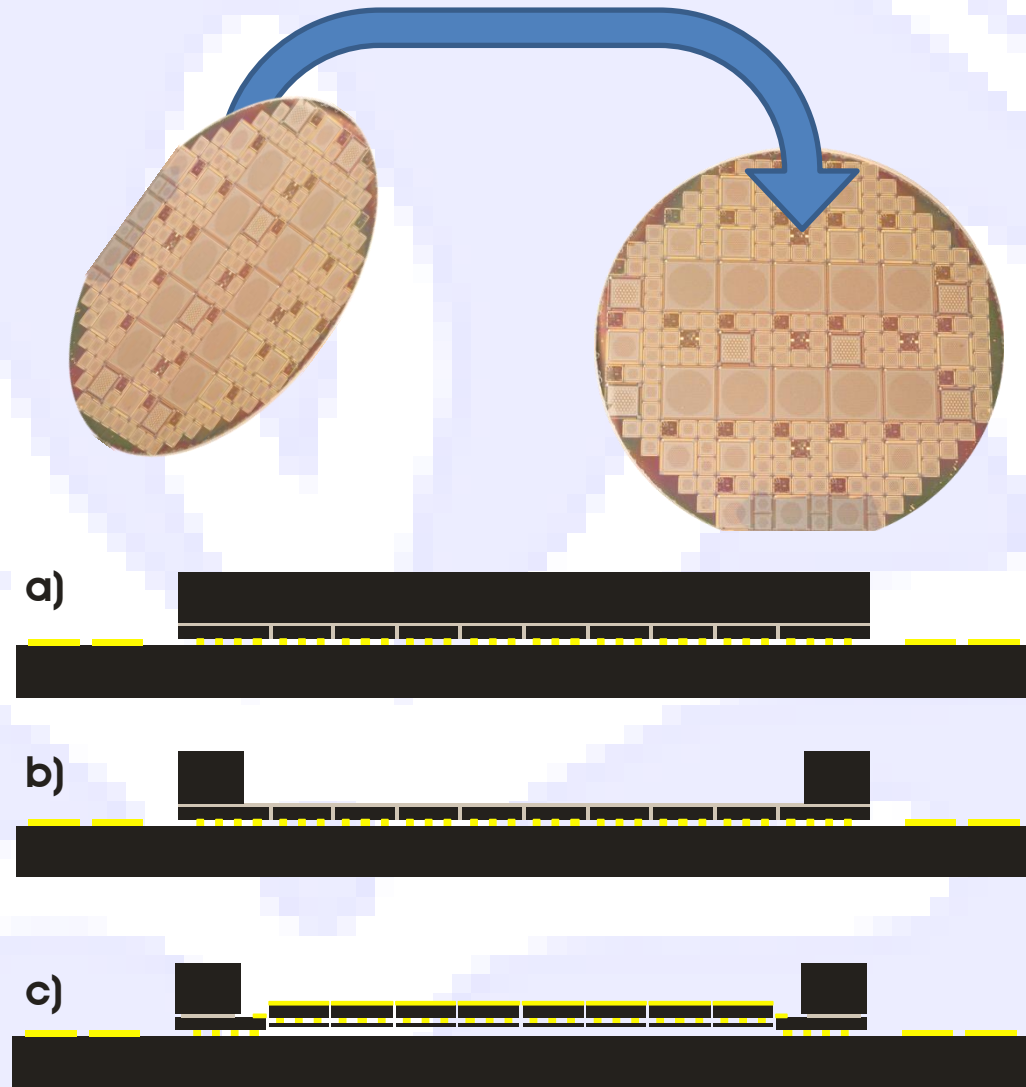
- Actuator and mirror wafer fabrication underway
 - Actuator wafers: ~30% completed
 - Mirror wafers: ~60% completed
- PTT939 process uses projection lithography
 - ASML PAS 5600/300 DUV stepper
 - Better uniformity
 - Excellent overlay error (layer-layer alignment)
 - $<0.1 \mu\text{m}$ observed
 - 0 mask defects
- Iris AO recently hired additional process engineers
 - Fabrication resources tripled
 - Crucial resources now available to focus on increasing yield
 - Initial studies have already resulted in a 15X reduction in defects



PTT939 DM Wiring Layer

Scaling Up: *Wafer-Scale Assembly*

- DMs >1000 actuators require wafer-scaled assembly techniques
- Wafer-scale assembly dramatically reduces effort to fabricate DM arrays
- Uses existing materials/designs Lowest risk path to wafer-scale assembly
- Two bondsite stacks compared
- Future testing will increase test-wafer complexity



Wafer-Scale-Bonding Destructive-Testing Results

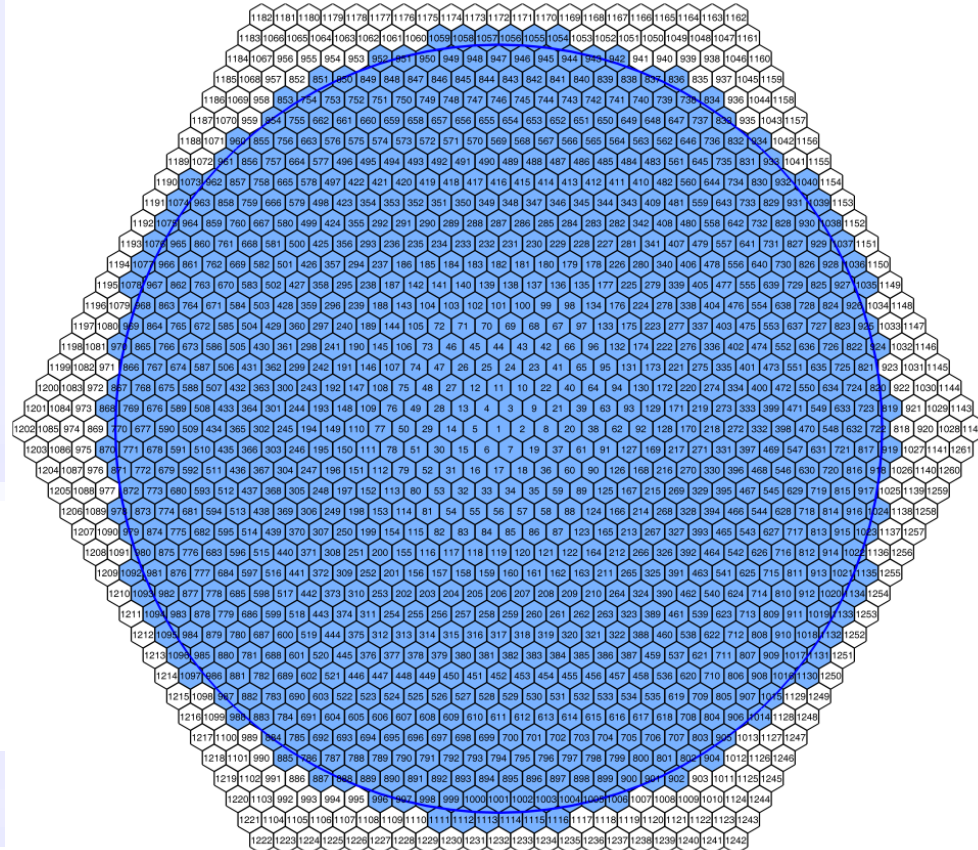


Phase I SBIR Development NNX16CD58P

Increasing Spatial Resolution Even More

Scaling to 3045 Actuators

- Design study of a 3045 actuator (1015 segment) DM
 - DM
 - Packaging
 - Electrical probe-testing hardware
- Results: All hardware is feasible using readily available technology
- Field-stitching demonstration for large arrays
 - Lithography system field size: 22mm x 27.4 mm
 - Excellent field-field alignment:
 - $3\sigma < 30$ nm reported
- PTT3045 design to be completed in Phase I
 - Design verification and fabrication in Phase II



PTT3045 DM

- 3045 Actuators
- 1015 PTT Segments
- 19.6 mm inscribed aperture

Summary

- Developing 20+ bit resolution drive electronics
 - Firmware completed, tests underway
 - Ultimate limit will be electronics noise floor and bandwidth requirements
- Fabricating a 1000 actuator DM – PTT939
- Developing wafer-scale assembly
 - Bond yield of early tests shows >90% yield across wafer
 - Enables scaling to 4th generation 1000 segment (3000 actuator) DM
- Designing 4th generation 3045 actuator DM