MEMS Deformable Mirror Development for Space-Based Exoplanet Detection

Iris AO, Inc.

NASA Phase II SBIR: NNX14CG06C

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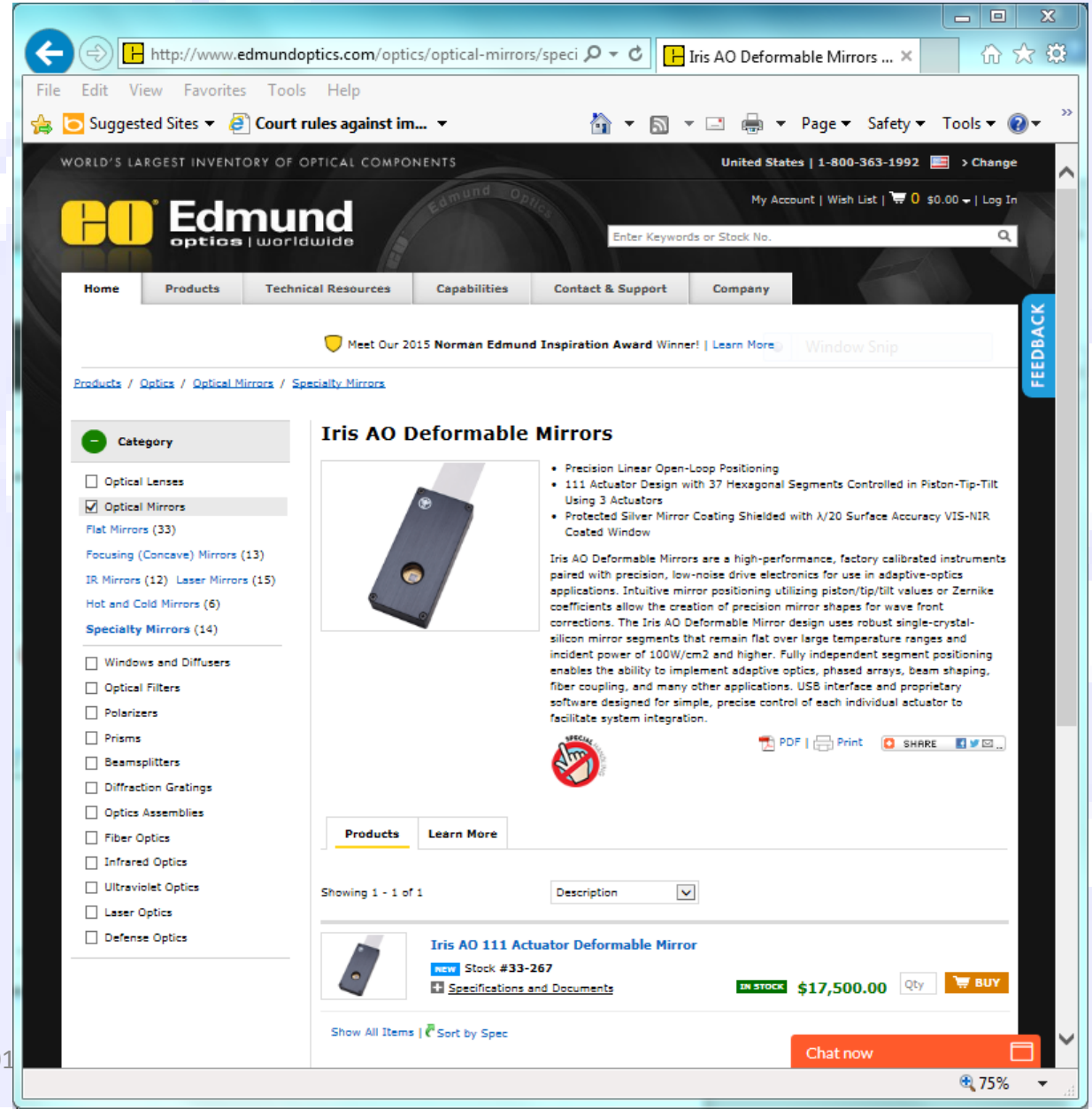
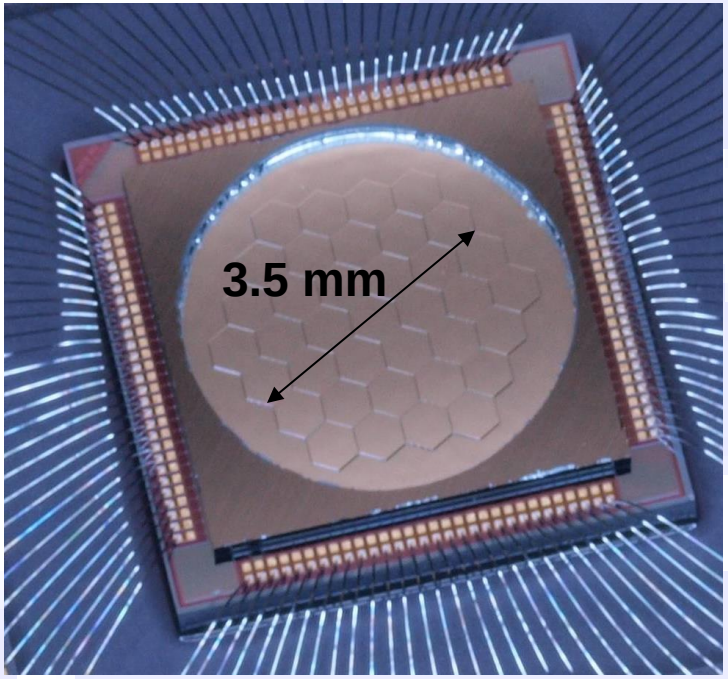
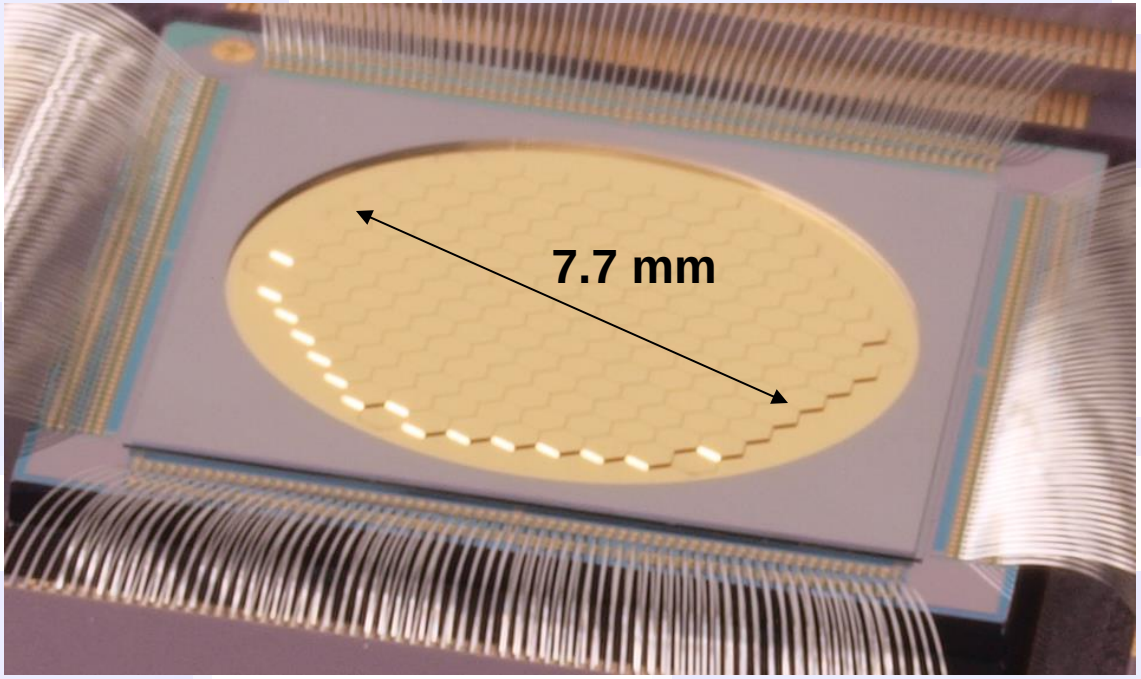
Iris AO PTT111 DMs Sold by Edmund Optics



Iris AO Segmented DM Background

Iris AO MEMS Segmented Deformable Mirrors

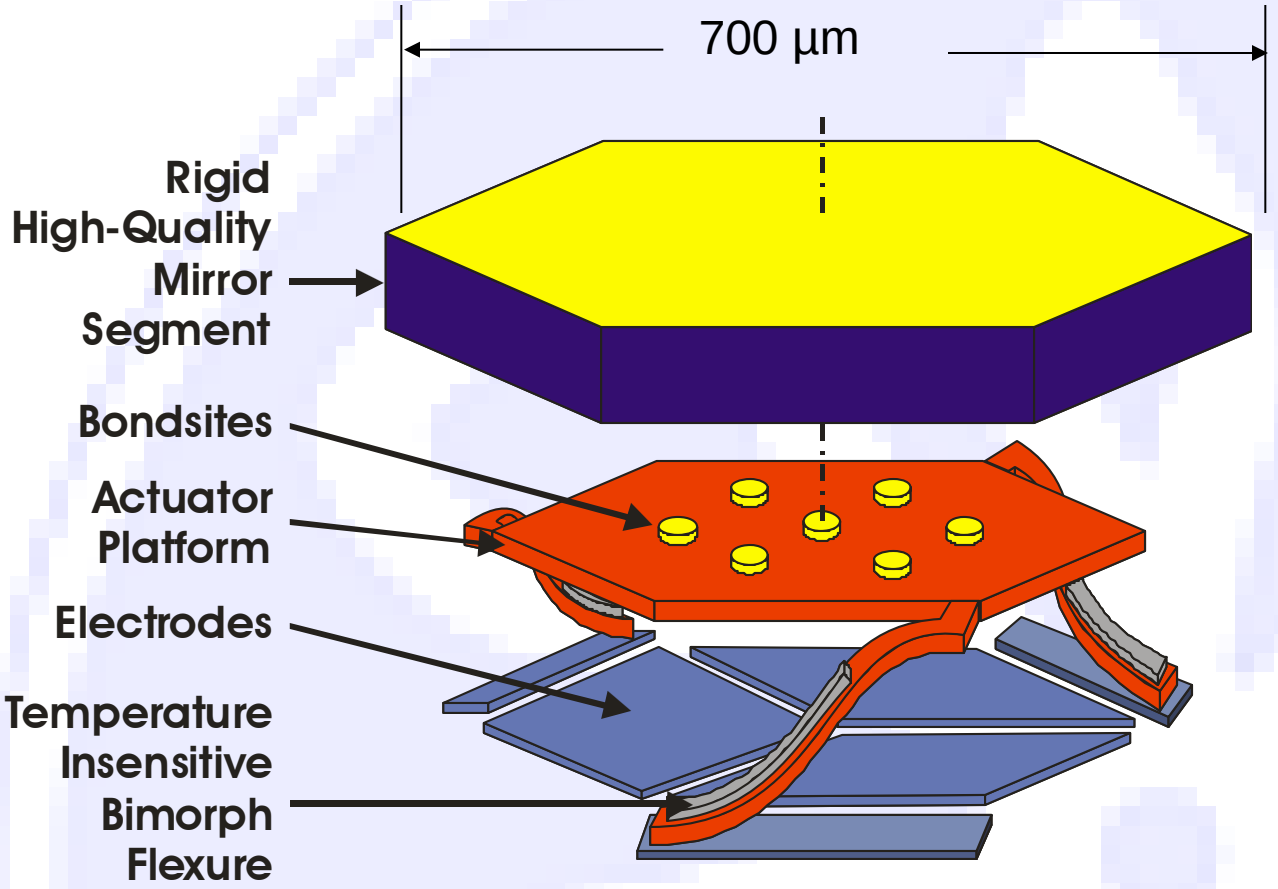




PTT111 DM
- 111 Actuators
- 37 PTT Segments
- 3.5 mm inscribed aperture
- Factory calibrated

PTT489 DM
- 489 Actuators
- 163 PTT Segments
- 7.7 mm inscribed aperture
- Factory calibrated

Iris AO Segmented DM Background



- 3 DOF: Piston/tip/tilt electrostatic actuation – no hysteresis
- Hybrid fabrication process
  - 3-layer polysilicon surface micromachining
  - Single-crystal-silicon assembled mirror
- Unit cell easily tiled to create large arrays
- Hybrid technology
  - Thick mirror segments
  - <1 nm PV/°C segment bow
  - Enables back-side stress-compensation coatings

Phase II SBIR Development NNX14CG06C

Critical Development for Manufacturing DMs for Exoplanet Detection

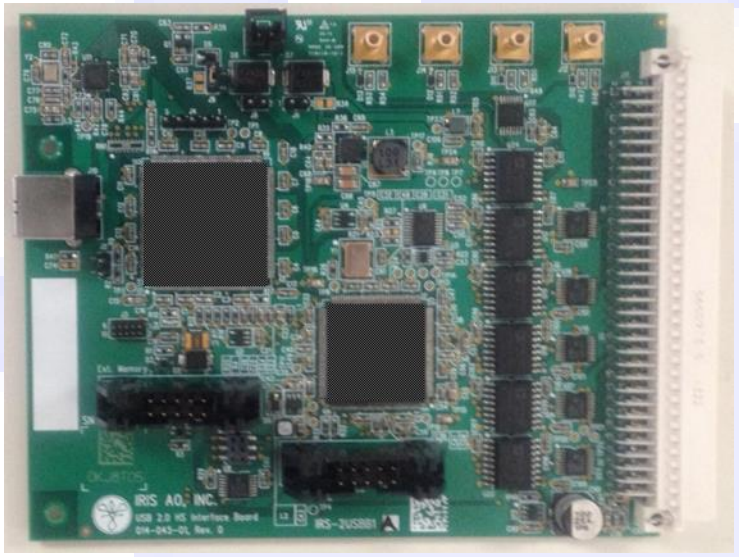
Electronics Development

- Standard Iris AO drive electronics are 14-bit resolution

NNX14CG06C Development

- 16-bit resolution HV driver card
  - Card built and preliminarily tested

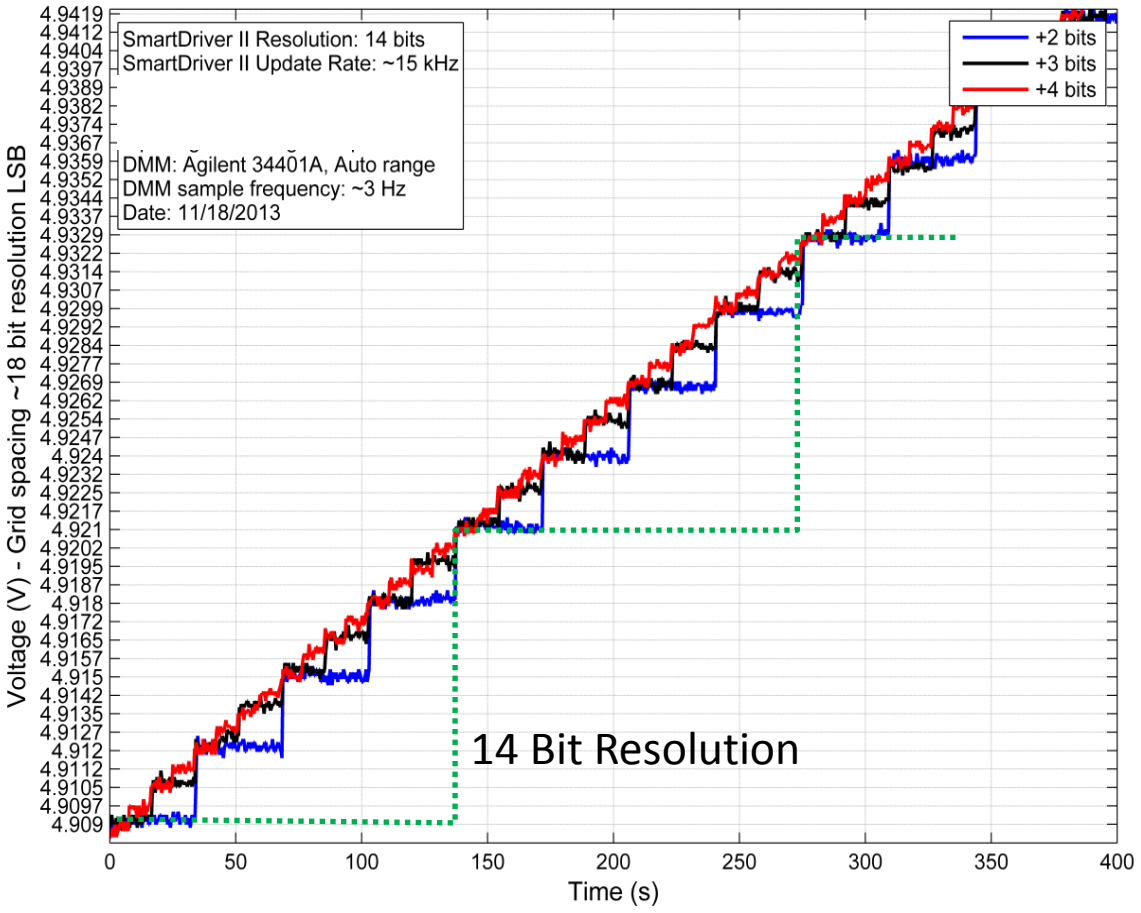
- USB2.0 High-Speed interface
  - Microcontroller
  - FPGA to implement timing critical modulation
  - Windows ***and*** Linux compatible
    - ~4 kHz updates under Linux



Super-Resolution Drive Electronics

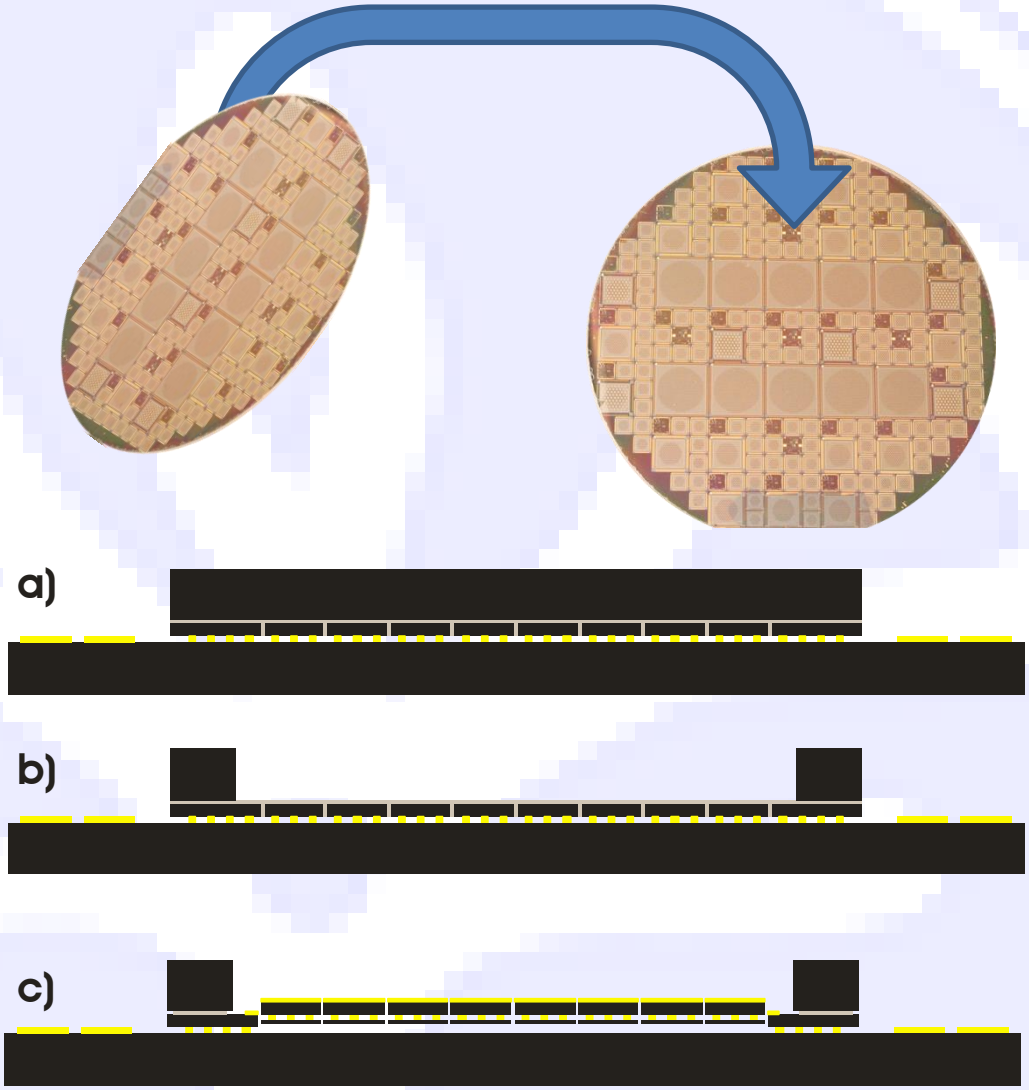
- Standard electronics are 14 bit resolution
- pm *rms* control will require >20 bit resolution
- Grid spacing is for 1 LSB on 18-bit resolution
- Super-resolution demonstration
  - +4 bits were demonstrated
  - Software driven control
- Phase II
  - 16 bit native resolution electronics
  - Modulation schemes implemented in FPGA
  - ***Expect 20+ bits of resolution***
- Testing to be complete Q1 2016

Software-Driven Super-Resolution Results



Scaling Up: *Wafer-Scale Assembly*

- DMs >1000 actuators require wafer-scaled assembly techniques
- Phase II development for thermo-compression bonding underway
  - Process development has lowered bond forces
  - Increased bond-tool tool capacity enables wafer-scale thermo-compression
  - Using existing materials/designs Lowest risk path to wafer-scale assembly
  - Alternative materials will be pursued in parallel
- Bonding runs to start December 2015

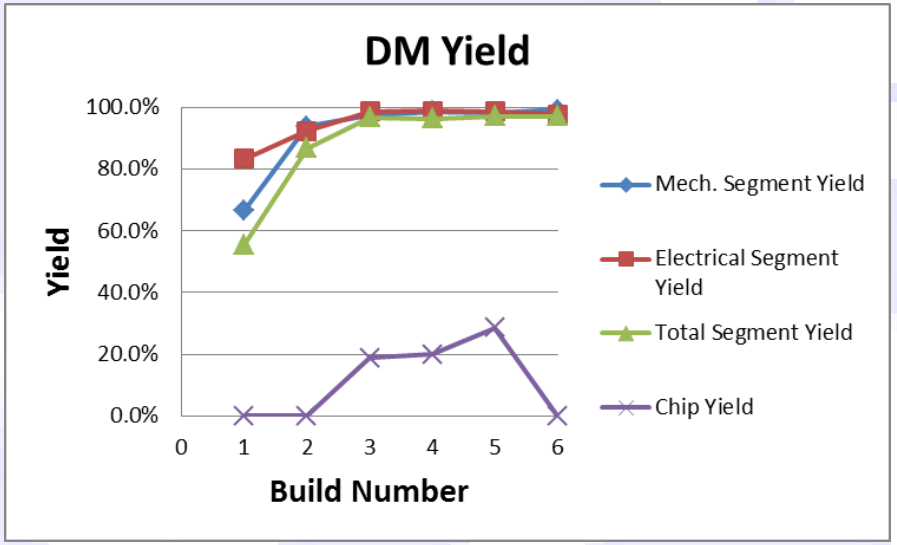


Yield Enhancement

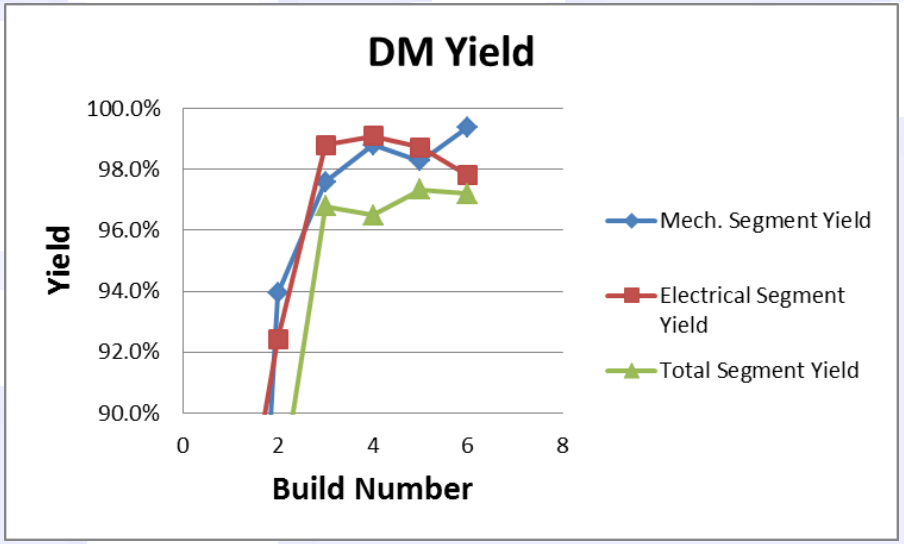
Results from 2014-2015 Yield Study
Mostly IR&D and some NNX12CA42C

DM Yield – 2014 Results

DM Build Number	Actuator Wafer Lot	Mirror Wafer Lot	Mech. Segment Yield	Electrical Segment Yield	Total Segment Yield	Chip Yield
1	PWA-02	LSM-01	66.8%	83.4%	55.7%	0.0%
2	PWA-02	LSM-02	93.9%	92.4%	86.8%	0.0%
3	PWA-03	LSM-02	97.6%	98.8%	96.8%	18.8%
4	PWA-03	LSM-02	98.8%	99.1%	96.5%	20.0%
5	PWA-03	LSM-02	98.3%	98.7%	97.3%	28.6%
6	PWA-04	LSM-02	99.4%	97.8%	97.2%	0.0%
7	PWA-05	LSM-03	TBD	TBD	TBD	TBD

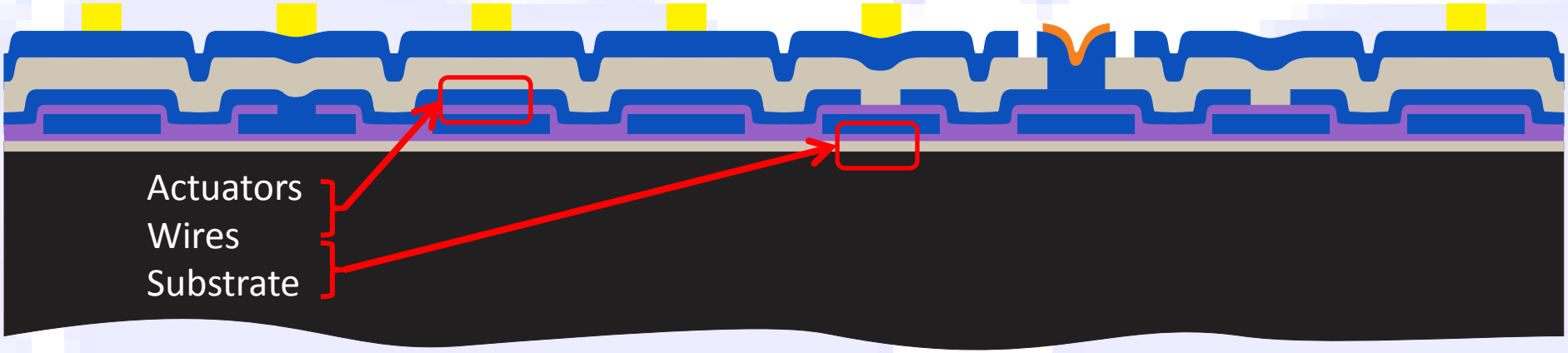


- Ideally yield increases monotonically with every fabrication lot
- Increased electrical short-circuit failures for PWA-04 actuator lot
  - Defects were more uniformly distributed rather than clustered
  - Result: 0% chip yield
- PWA-04 lot had thicker passivation layers and more aggressive anneal schedule



Fabrication-Process Investigation

- Starting Hypotheses
  - Random event: Poor film quality isolated to the particular fabrication run
  - Systematic event: “Minor” process changes in PWA-04 lot resulted in devastating effects
    - Thicker passivation layers
    - More aggressive anneals



Short-Loop-Test Results

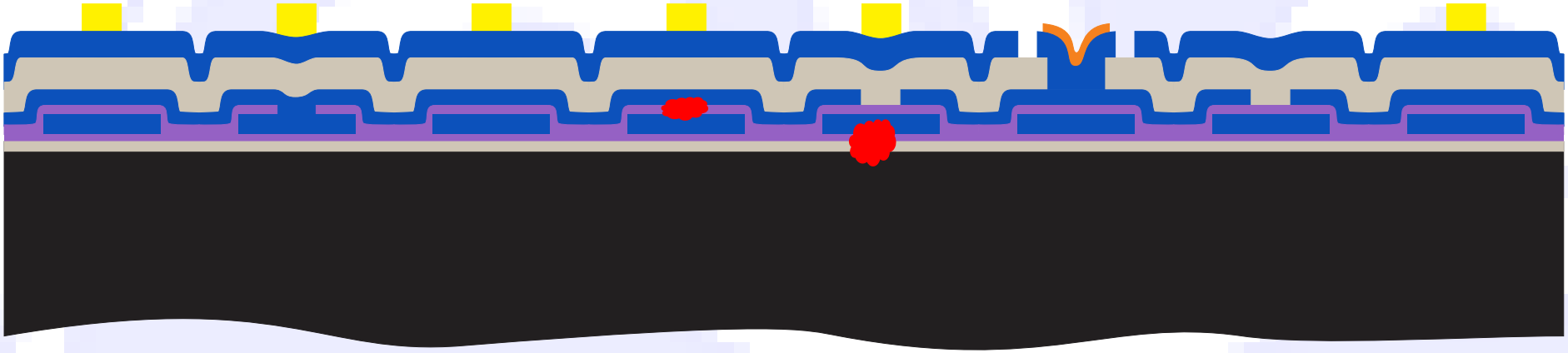
- Short-loop test was run to attempt to test hypotheses
  - Short-loop: subset of the fabrication process
  - Same masks used as PWA-04 lot
  - Wafer splits
    - Same layer thicknesses as PWA-04 lot
      - aggressive anneal schedule
      - reduced anneal schedule
    - Same process as PWA-03 lot
- Results
  - Consistent with prior runs
    - Excessive short circuits spread across wafer
    - PWA-03: Enhanced breakdown at 200 V
    - ***Process is repeatable!***
  - Excessive failures tracked to defects in the photolithography masks
    - Defects track with chip ID/location
  - Anneal schedule had no affect

PWA-05 Actuator Fabrication Run

- New masks to “eliminate” mask defects
- Process splits – to show repeatability
  - PWA-03 layer stack
  - PWA-04 layer stack
- Results
  - Reproduced results from PW-03 and PWA-04 wafer lots but with increased yield
  - Even with new masks, 34% of short-circuit failures attributed to mask defects
    - PTT489 chip-yield would be ~2X greater if these defects were eliminated
  - Electrical yield appears to be a function of the design of upper layers unrelated to the wiring and actuators
  - Chip yield could be increased ~3X with projection lithography and the best design!
- **Conclusions**
  - ***The actuator-wafer fabrication process is repeatable***
  - ***Future runs should use projection lithography system***

Contact-Lithography Mask Defects

- Defects in masks expose areas of wafer when etching passivation (insulator) layers
- Subsequent wire or electrode layer deposition over defects causes short circuits



- Solution
  - Projection lithography system with 4:1 reduction
  - Masks do not touch the wafer
  - Masks are machine inspected to guarantee 0 defects >0.5 µm
    - Smaller than what is resolvable on wafer after reduction

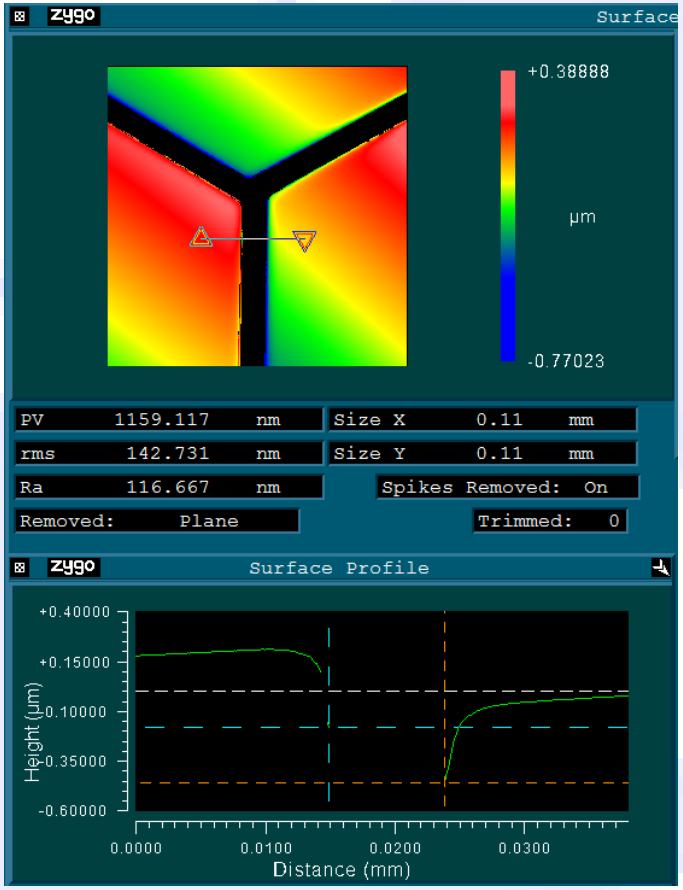
Next Steps

- Continue to mature the DM fabrication and design
  - Improve mirror-assembly yield
    - Build 7 DMs had large yield reduction caused by an issue with mirror-assembly process
  - Implement best practices on next generation DMs
    - Highest-yielding design
    - Projection lithography system

Improved Segment Gaps

NSF Phase II SBIR IIP-1152710

PT111 Segment-Gap Reduction

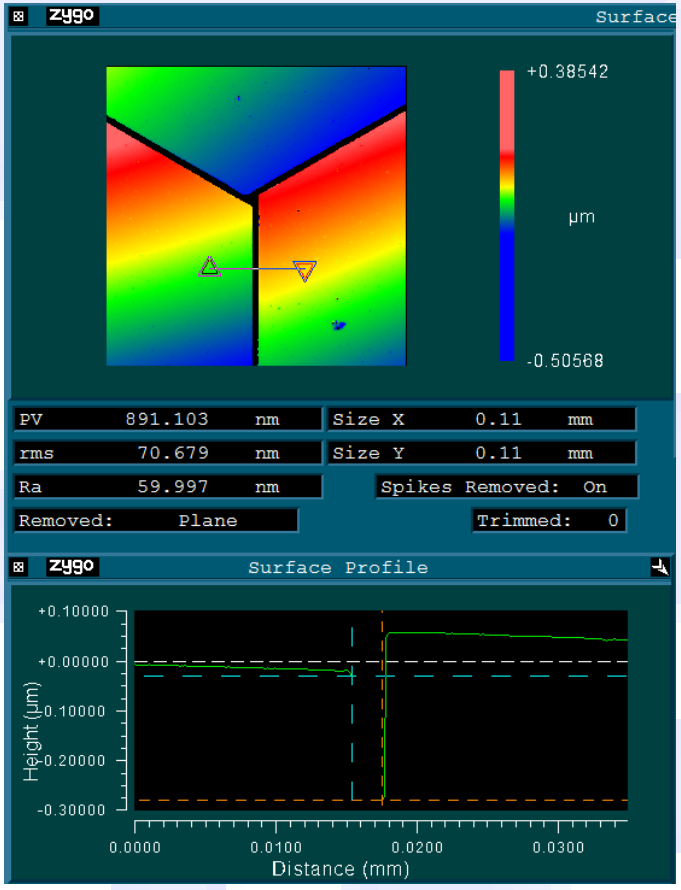


2nd Gen. PTT111 DM Mirror Gaps

Gap: 9.0 µm → 98.5% Fill Factor

Edge Roll Off: 0.4-0.5 µm

Gap + Roll Off → 96.7% Fill Factor



3rd Gen. PTT111 DM Mirror Gaps

Gap: 2.2 µm → 99.6% Fill Factor

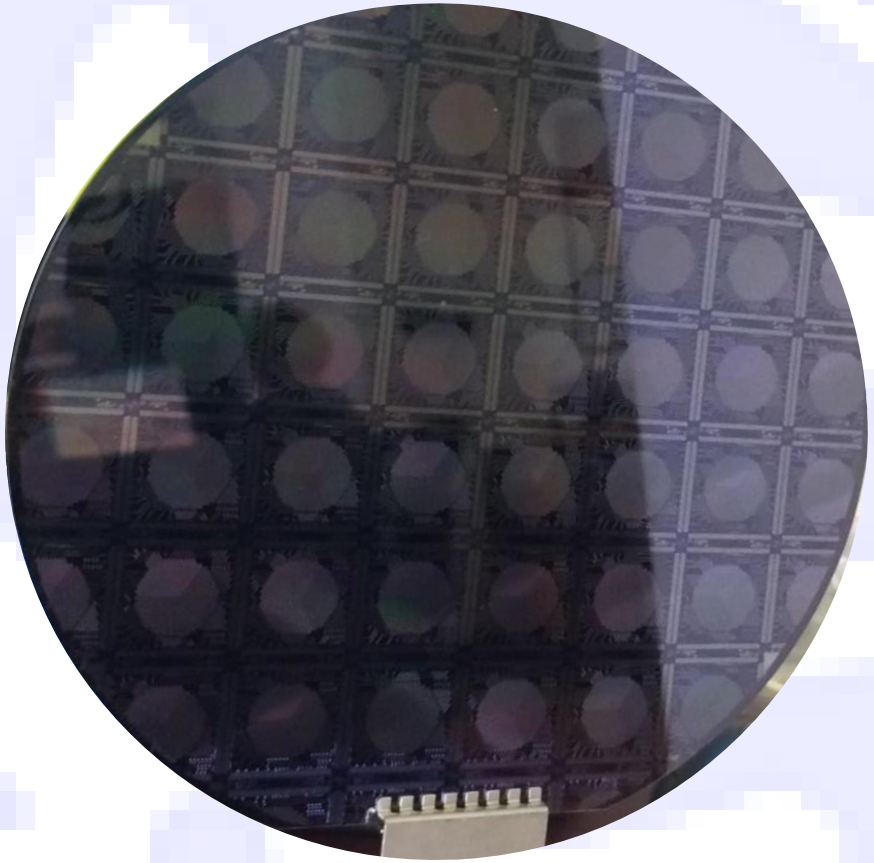
Edge Roll Off: 0.4-0.5 µm

Gap + Roll Off → 99.5% Fill Factor

PTT939 Fabrication Run

Scaling up to ~1k Actuators (PTT939)

- Designs complete for PTT939 DM
- 50% of the masks for actuator wafers are in house
- Short-loop tests validated masks and DUV stepper lithography system
- Full fabrication run to start ~January 2016



PTT939 (Partial) Actuator Arrays on a 6” Wafer

Outlook for 2016

- Environmental testing for PTT489s
  - Shock/vibration, acoustic
  - Test DMs after recent radiation testing
- PTT489 DMs with smaller gaps
- PTT939 fab process completed

Summary

- Developing 20+ bit resolution drive electronics
- Wafer-scale assembly under development
  - Enables scaling to 4th generation 1000 segment (3000 actuator) DM
- Major yield improvements
  - Defects on PWA-04 run determined
  - Higher actuator yields demonstrated on PWA-05 run
  - Dramatic chip yield improvement (3X) possible
    - Projection lithography
    - Use best design
- Segment gaps reduced to ~2.2 µm on PTT111 DMs
- Design of 3rd generation 1000 actuator DM completed
  - projection lithography tested by patterning a wafer with actuator wiring layer